A NEW FAILURE MECHANISM BY SCANNING ELECTRON MICROSCOPE INDUCED ELECTRICAL BREAKDOWN OF TUNGSTEN WINDOWS IN INTEGRATED CIRCUIT PROCESSING

BY

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A NEW FAILURE MECHANISM BY SCANNING ELECTRON MICROSCOPE INDUCED ELECTRICAL BREAKDOWN OF TUNGSTEN WINDOWS IN INTEGRATED CIRCUIT PROCESSING

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As device dimension steadily decrease in integrated circuit manufacturing, the use of scanning electron microscopy (SEM) has increasingly replaced optical microscopy for defect detection and defect analysis. Yet, the interactions between the electron beam, the surface scanned, and the further processing of the die is relatively unknown. A project was undertaken to determine what, if any, implications SEM imaging of an in-process wafer had on the electrical integrity of the scanned areas. Attention was focused on the window and via modules.

Three SEMs currently in production use were utilized. Two wafers were processed to dielectric one. SEM imaging was performed on window-1 stitches to P+ and N+ source/drain contacts as well as window-1 to gate contacts. The points in the processing where SEM scans took place were after window etch, after window liner deposition, after window-1 tungsten CMP, and after metal-1 etch. The metal-1 was intentionally misaligned in order to expose the tungsten plugs. One wafer then received a solvent clean and one wafer received no clean The resistance of the source/

drain stitches increased significantly up to and including electrical opens, for those structures that were scanned by all three SEMs. The structures that were scanned by only a single SEM did not deviate significantly from the control. The measured resistances were somewhat lower than for the wafer that received the solvent clean as compared the skip clean wafer, but the values did not approach the control cell levels.

Additionally, window-2 stitches and Kelvins were scanned with the SEMs after overlying metal etch with misalignment. One wafer each then underwent post-metal-etch cleans by a neutral solvent, an alkaline solvent, an acidic solvent, and one wafer received no clean. No deviations from the control cell resistances were measured

CHAPTER 1
INTRODUCTION

As the integrated circuit (IC) industry has rapidly expanded over the last three decades the processing demands for IC manufacturing continually drive toward building smaller, faster, cheaper and yet more complex microchips, in accordance with Moore's law. In 1964, Intel cofounder Gordon Moore predicted that integrated circuit density would double every eighteen months.[i]

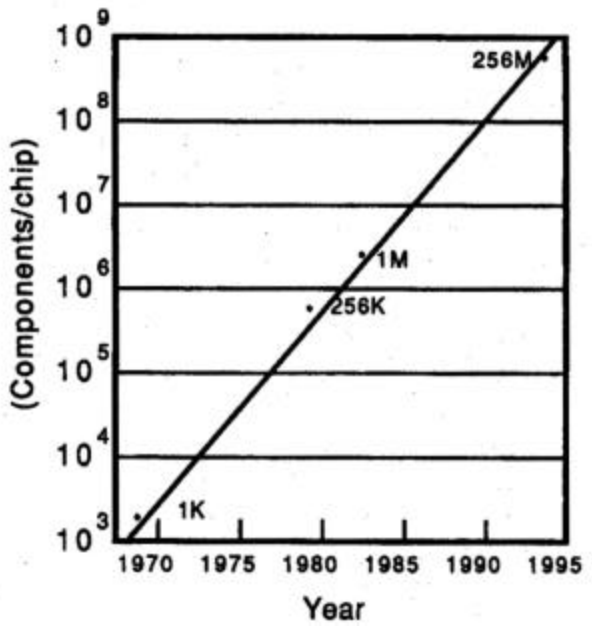

Figure 1. DRAM Density Growth by Year.[i]

As can be seen in the figure of DRAM density by year, this prediction proved accurate. Currently, the most complex microchips being manufactured contain over 100

million transistors on a single die. The ultimate goal of manufacturing is to produce functional chips at continually higher volume and lower cost. Improvements in functional volume can be achieved by increasing wafer size, by decreasing die size through decreased critical dimensions, or by designing ICs for manufacturability with an eye toward a reduction in critical area.

The most productive method, however, for improving the functional die output is by improving the total die yield. Die yield is the percentage of total die successfully manufactured, from silicon processing all the way through packaging and testing. Die yield is a function of manufacturing yield, test yield, package yield, and occasionally burn in yield. Since test, package, and burn in yield are typically close to unity, the die yield effectively becomes the manufacturing yield.[ii] For a given technology, reductions in defect density improve manufacturing yield. As technologies shrink, feature sizes decrease, and as feature sizes decrease, the size of a defect that can cause a functional failure decreases as well. For example, a 0.25µm piece of dirt that falls between two metal runners separated by 1.0µm of space will most likely not be detrimental to the chip. If, however, that same 0.25µm piece of dirt falls across adjacent metal runners separated by a 0.25µm space, that piece of dirt could become a killer defect destroying the entire chip.

There are only four basic operations required to produce an integrated circuit: layering, patterning, doping, and heat treatment. In modern IC processing these four steps are repeated in over two hundred discrete processing steps in an infinite number of combinations, and each one of these steps are potential defect contributors that can reduce the total yield.[ii] One estimate suggested that particles are responsible for 75% of

total yield loss in volume IC manufacturing.[iii] Defect inspection, defect classification, and defect source identification are a crucial part of every modern IC fab. By necessity, advances in particle detection technology have kept pace with overall technology development.

There are two types of in-process optical particle detection. The first type is optical scattering of a laser beam as it scans the surface of a blank wafer. The inspection station takes measurements of blank wafers before and after the process of interest, using a surface particle counter that records the quantity of added particles as well as their location on the wafer. The smallest reliably identifiable particle size detectable depends greatly upon the type of surface scanner, the shape and refractive index of the particles, and the wavelength of the beam used. In general, the sensitivity falls off rapidly below particle sizes of approximately 0.20µm. The second type of optical defect inspection is used with product wafers. These systems use the repeating pattern of the die as a template for comparison. The inspection station records locations and approximate sizes of areas with significant differences in comparison to their adjacent flash. While these systems generally have less sensitivity and lower throughput, they are much more flexible and have the advantage of being able to detect additional defect mechanisms, such as patterning defects and corrosion, that the laser scanning systems do not.[ii]

In either case operators, then use scanning electron microscopes (SEM) to analyze the recorded defects, using the generated defect maps as their guide. The SEM inspection can determine the type of defect, the source of the defect, and compositional construction if equipped with x-ray detection systems. This knowledge is used to determine corrective actions both for the analyzed wafer lot and future wafer lots. SEMs have virtually

replaced optical microscopes as the tool of choice for analysis as critical dimensions have shrunk beyond the 0.25µm generation into the 0.18µm, and 0.15µm generations, and will be increasingly relied upon in the 0.13µm generations and beyond. The reasons for this are obvious: the shortest wavelengths of visible light, even in the lowest end of the spectrum in the blue and violet range, are in the 400-450 nanometer range – two to three times larger than the physical dimensions of the smallest features currently being printed. The critical dimensions of IC manufacturing have exceeded the resolution limits of optical microscopy. On the other hand, SEM technology can readily resolve features down to 10nm, with depths of focus equivalent to optical microscopy. In addition to post inspection analysis, recent SEM hardware developments have begun a migration away from optical to SEM based defect detection systems. In these new e-beam detection systems, defects are located as in the optical systems, but in addition, there is a new capability of finding defects based on their electrical activity; a rudimentary in-process non-destructive electrical test. Essentially, electron impingement on the surface of the wafer induces a voltage on the surface. Local electric fields at the sample surface impact the number of electrons coming off that surface which influences the resultant image. If, however, a structure under electron beam inspection has a path to ground that structure will not charge, resulting in an image contrast in comparison to a floating feature in the same field of view. An example of this "voltage contrast" image is seen in Figure 2, which is a top-down SEM image of a window stitch. The point at which the overlying

metal pads transitions from bright to dark indicates a break in electrical continuity.

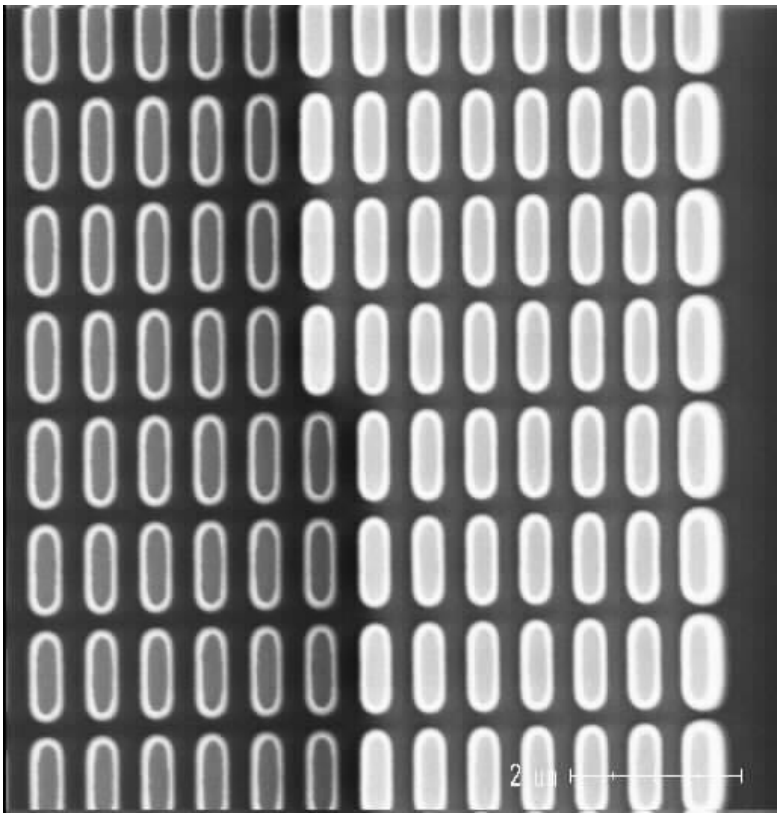

Figure 2. SEM Image of Window Stitch Indicating Voltage Contrast of Electrical Open

A second example of voltage contrast is seen in Figure 3, a top-down SEM image of adjacent metal runners. These adjacent runners should alternate between being electrically floating and electrically grounded, however, a section can be seen where every runner is bright indicating shorting between adjacent runners. This voltage contrast phenomenon is now being used inline in volume manufacturing, within the process flow, non-destructively to isolate both electrical shorts and opens. Previously undetectable defects are now being detected inline, at the point of failure, saving time and money.

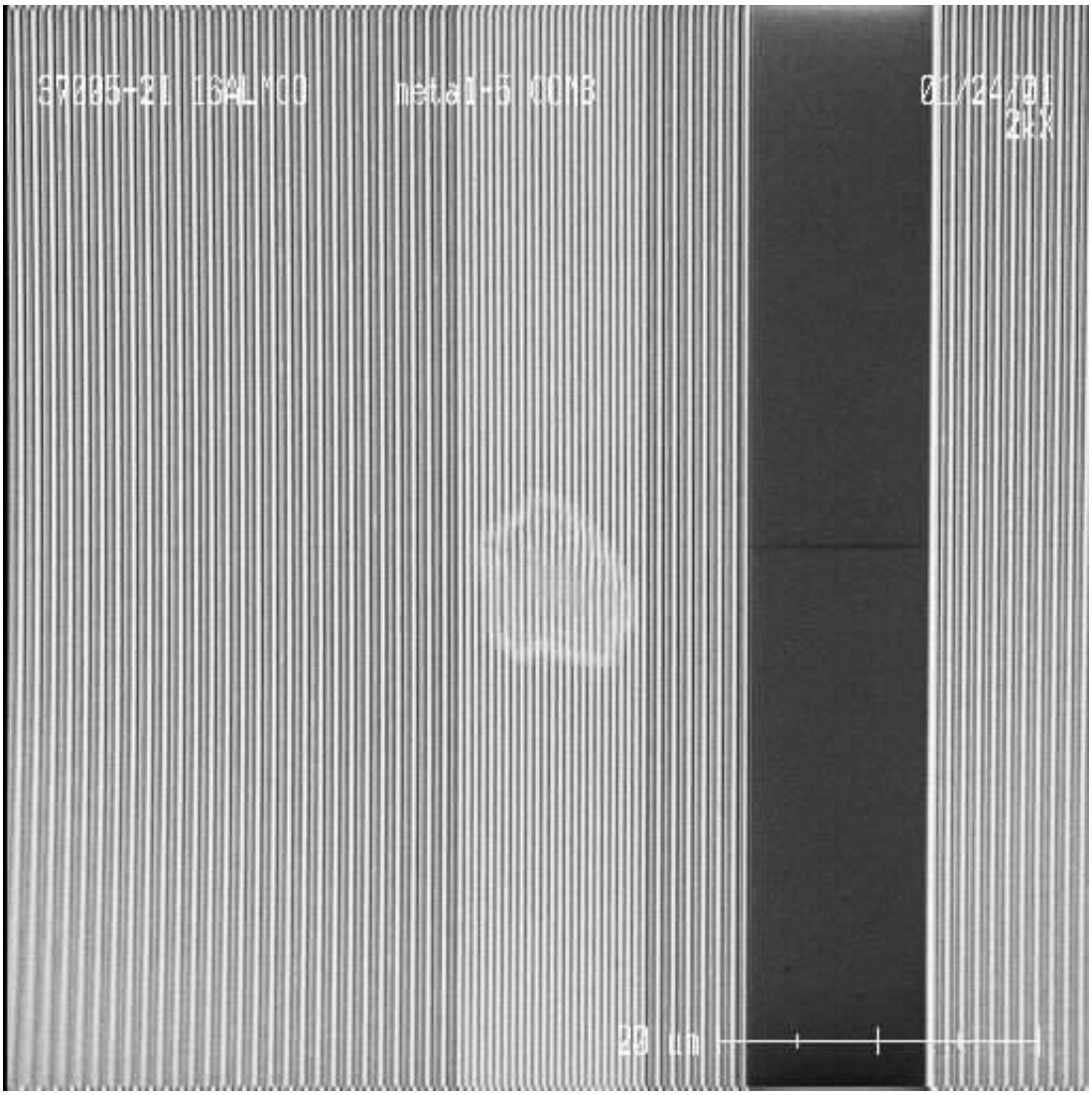

Figure 3. SEM image of Metal Runners Indicating Voltage Contrast of Metal Short.

Since the use of scanning electron microscopes are ubiquitous throughout the manufacturing of integrated circuits, of obvious concern is any impact that SEM inspection imposes on the processing. The SEM can be used before or after almost every one of the more than two hundred steps in a typical process flow. It is an electron beam that interacts with metals and oxides, it induces charges on the surface being inspected, it can break bonds, and it can deposit a thin layer of carbon onto the surface being imaged.

While the SEM is being used for yield improvement it must be established that it is not, in fact, contributing to yield loss by inducing defects.

A recent instance indicated the SEM might have been a source of defectivity. In this case, a field of window-1 tungsten plugs was inspected for defects after window-1 chemical-mechanical polish (CMP). As can be seen in Figure 4, the defective window-1 plugs are dark, whereas the good plugs are bright. There are two defects visible, separated by approximately five columns of plugs. After SEM inspection the wafer was cleaned as a normal matter of process flow It was then discovered that where the SEM beam had imaged the defect, some of the tungsten plugs that were previously unflawed were now defective.

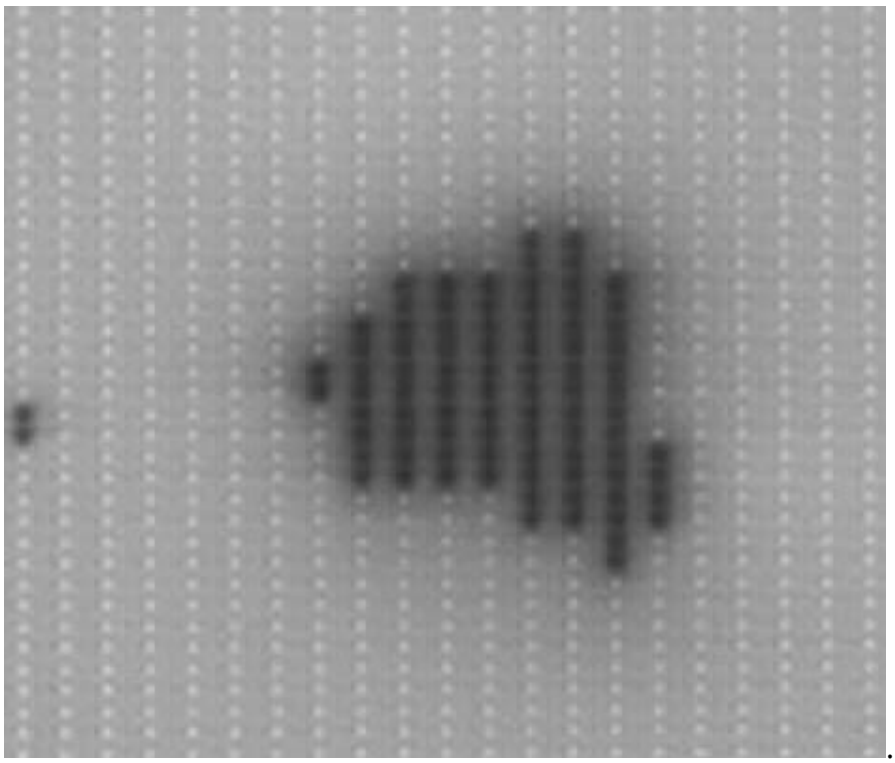

Figure 4. Random Processing Defect At Window-1 Level, After Tungsten CMP

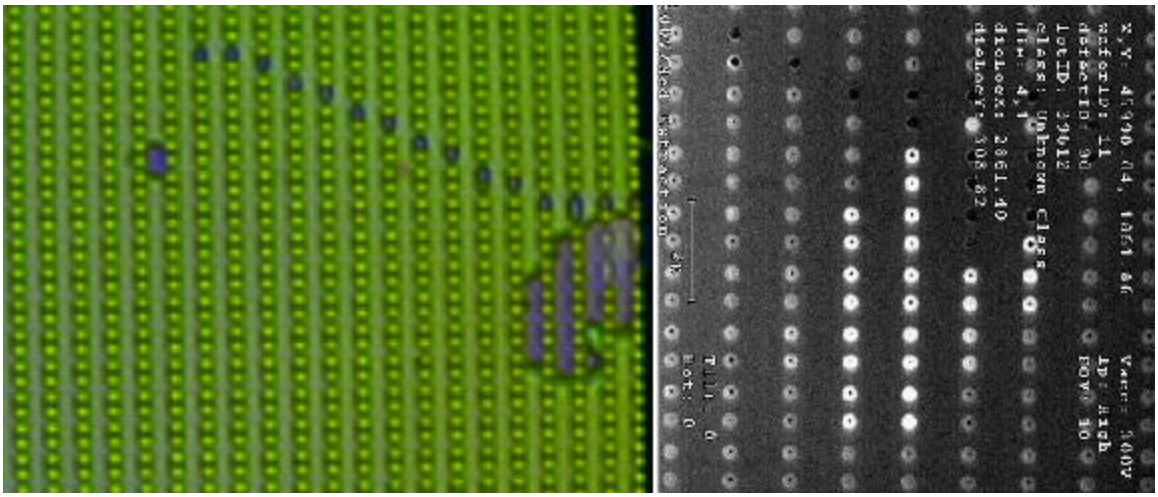

Figure 5. Same Defect as Figure 4, after Post-SEM Clean: Cored Tungsten Plugs where SEM Beam Impinged (Optical and SEM Images.)

A square of cored out tungsten plugs is visible over the large defect, and a path of missing tungsten can be seen where the SEM traveled from the first defect to the second. It appeared that the SEM had induced damage.

The purpose of this study was to determine whether, in the process of locating and inspecting defects in integrated circuit processing, the SEM interacts with the sample causing defects where none prior existed. In the first analysis, simple window-1 chain structure were scanned with electron beams. Three different SEMs were utilized at four points in the process on five different flavors of window-1 stitches. These wafers were then pulled out of line after the metal-1 step, and analyzed. In the second analysis, window-2 stitches and single contact window-2 Kelvin structures were scanned with electron beams. In this case, three different SEMs were utilized at only one point of the process, then three different post-metal-etch cleans commonly used in IC manufacturing were employed, in order to investigate SEM-cleans interactions. These wafers were pulled out of line after metal-2 patterning, capped and analyzed.

The focus of this study was on the window module – the electrical contact between metal-1 and gate, N-doped source/drain, and P-doped source/drain, and between the electrical contacts connecting metal level to metal. It was found that scanning electron microscope imaging of in-process wafers induced electrical failure of the window-1 to source/drains. In-process SEM scanning of window-1 to gate contact was also found to increase the overall resistance of a gate contact structure, but did not cause catastrophic failure of that structure. Finally, in-process SEM scanning of window-2 between metal-1 and metal-2 did not find any perturbation of the electrical characteristics of the window-2 structures, regardless of the method of clean employed after the SEM imaging. It is speculated that the root cause of the electrical fail falls into one of three categories

- The SEM imaging of the surface deposits a thin interfacial film of carbon that disrupts electrical continuity
- The SEM disrupts the normal deposition of thin films, or the normal structural integrity of thin films
- The SEM imposes a stored charge on the sample surface, that upon subsequent processing, drives electrochemical/galvanic corrosion of one of the metal thin films.

Cross-sectional scanning transmission electron micrographs as well as top-down scanning electron micrographs of the high resistance window structures did not conclusively determine the root cause of the electrical failure, however there is some evidence to at what point in the IC processing the damage occurred.

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CHAPTER 2
SEMICONDUCTOR PROCESSING: BACKGROUND AND REVIEW OF LITERATURE

2.1 Processing

2.1.1 The Manufacturing Flow

The method used to manufacture integrated circuits on silicon wafers is the fabrication of successive layers of patterned conductors, semiconductors, and insulators. Beginning with an eight inch lightly P-doped silicon wafer starting material on which epitaxial silicon has been grown, shallow trench isolation (STI) is patterned and etched. An oxide layer is then deposited to fill the trenches, using a high density plasma enhanced chemical vapor deposition (HDP-CVD) process. The advantage of HDP-CVD is the ability to perform in-situ simultaneous deposition and sputter etch of oxide films which improves the oxide gapfill of high aspect ratio spaces, in comparison with standard CVD oxides.[iv] Chemical-mechanical polishing is used to polish back the oxide to maintain planarity, followed by a megasonics brush scrub cleans. Next, ion implantation defines the tubs. Because this technology features two voltages, a total of four tubs are required – 1.5V Ntub, 3.3V Ntub, 1.5V Ptub, and 3.3V Ptub. Subsequently, thermal oxidation of the epi-silicon grows the high quality gate oxide. Then, low pressure CVD is employed to deposit an amorphous layer of silicon that becomes the first layer of the two-layer gate stack. This amorphous silicon layer is implanted, activated by rapid thermal anneal, capped with a sputtered tungsten silicide layer to lower sheet resistance,

and patterned. Next, phosphorous and boron implants define the N-doped and P-doped sources and drains for both voltage specifications. At this point, HDP-CVD is again used to deposit a few thousand angstroms of oxide, followed by a rapid thermal anneal to activate the implants and anneal out any lattice damage incurred in the epitaxial silicon sustained by ion implantation. Plasma-enhanced CVD of a phosphorous doped dielectric, using tetra-ethyl-ortho-silicate (TEOS) as the precursor, caps the HDP oxide. CMP achieves planarization of the wafer, as it polishes back dielectric-1 to its final thickness, and the wafer is cleaned. Next photolithography defines window-1 and a plasma reactor etches it. The wafer is plasma cleaned and rinsed with de-ionized water, and the window-1 stack is deposited. Window-1 plug consists of a titanium glue layer, and a titanium nitride barrier layer underneath a tungsten slab. Next, tungsten CMP polishes away the blanket tungsten leaving only the tungsten filled plugs, and the wafer is cleaned again. Metal-1 is sputter deposited as a multi-layer stack consisting of a titanium/titanium nitride (Ti/TiN) barrier, aluminum copper alloy conductor, and a titanium nitride (TiN) anti-reflective coating used for improved photolithography and as an etch-stop for window-2 etch. A representation of the processing to this point can be seen in Figure 6.

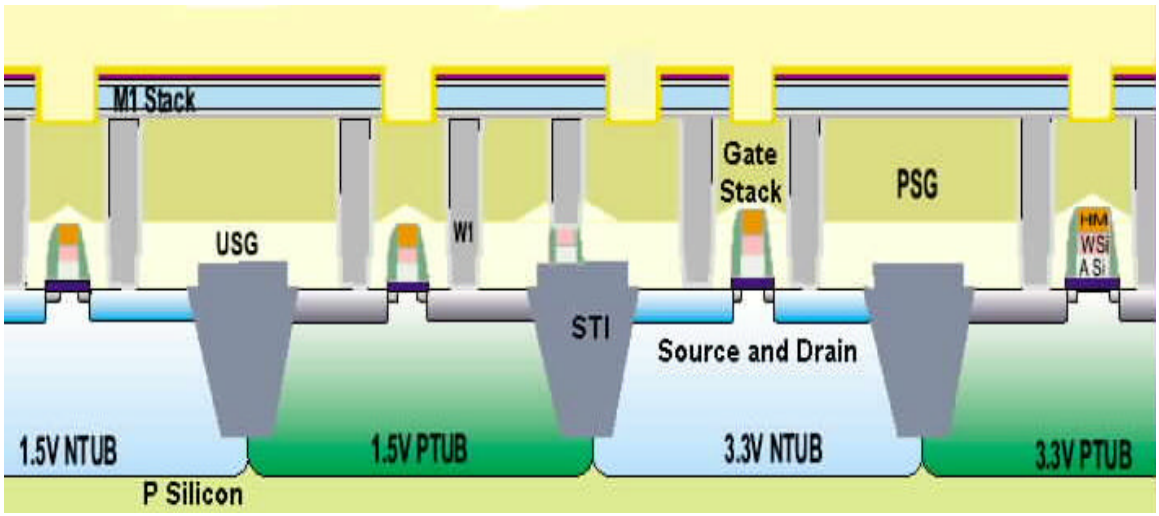

Figure 6. Process Cross-section Representation Through Metal-1

From this point on, the back end is a repetition of the previous steps, namely interlevel dielectric deposition, oxide CMP, window pattern and etch, tungsten deposition and CMP, metal deposition and patterning. This process repeats to form the multi-level metal schemes that can stack seven or more levels on the most complex chips. A cross-sectional representation of a fully processed five-level metal die can be seen in Figure 7.

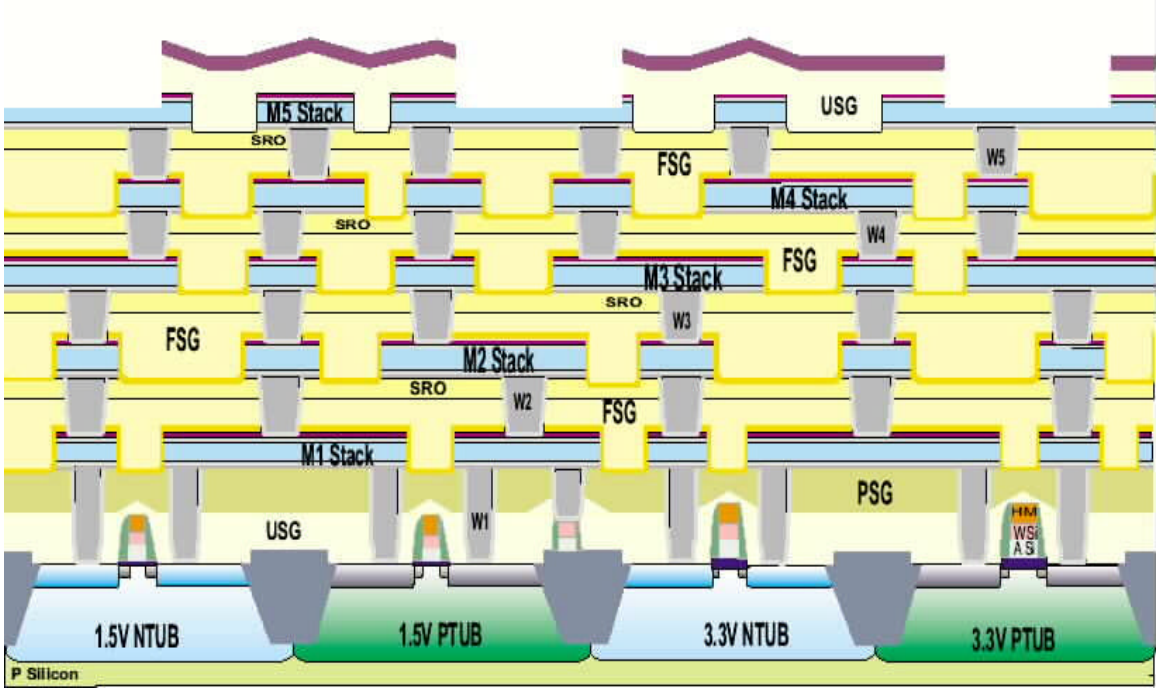

Figure 7. Five Level Metal Microchip Process

Figure 7 is an idealized representation showing perfect processing. In reality such parameters as alignment of one layer to the next, linewidth of the various features, and thickness of the metal and dielectric stacks will not be perfectly achieved. This variation is accounted for and defined by design rules that specify targets and allowed variation, usually defined as a 3 sigma or 4 sigma variation, for linewidth, thickness and every other imaginable and measurable parameter. At process technologies greater than 0.25µm , the design rule for the minimum metal overlap of the via is large enough to assure that the via plug does not fall off the underlying metal, nor does overlying metal expose the tungsten plug even at the worst case critical dimension variation and misalignment of the metal lines and vias. Increasing demands on the metallization system to provide the maximum density possible at the 0.25µm node and beyond require that contacted metal pitch be minimized to the point that metal to via to metal overlap design rule are reduced to zero.[v] Figure 8 highlights these borderless contacts due to reduction in metal pitch

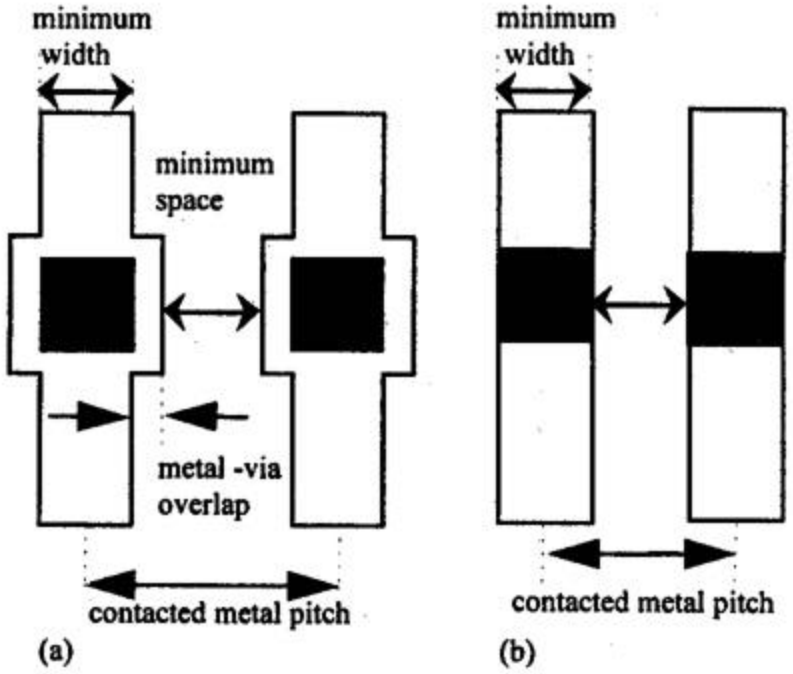

Figure 8. Contacted Metal Pitch Reduction By Zero Overlap Design Rules (a) metal-via overlap (b) zero metal-via overlap[v]

Such an approach, however, leads to the vias falling off the metal due to misalignment and variation in critical dimensions that are allowed by the design rules. At the end of metal lines, where end of line shortening and line rounding occur, this exposure of tungsten to further processing is exacerbates these borderless contacts. Figure 9 illustrates how this allowed misalignment will lead to exposure of the tungsten plugs to metal etch, post-metal etch cleans, and dielectric deposition.

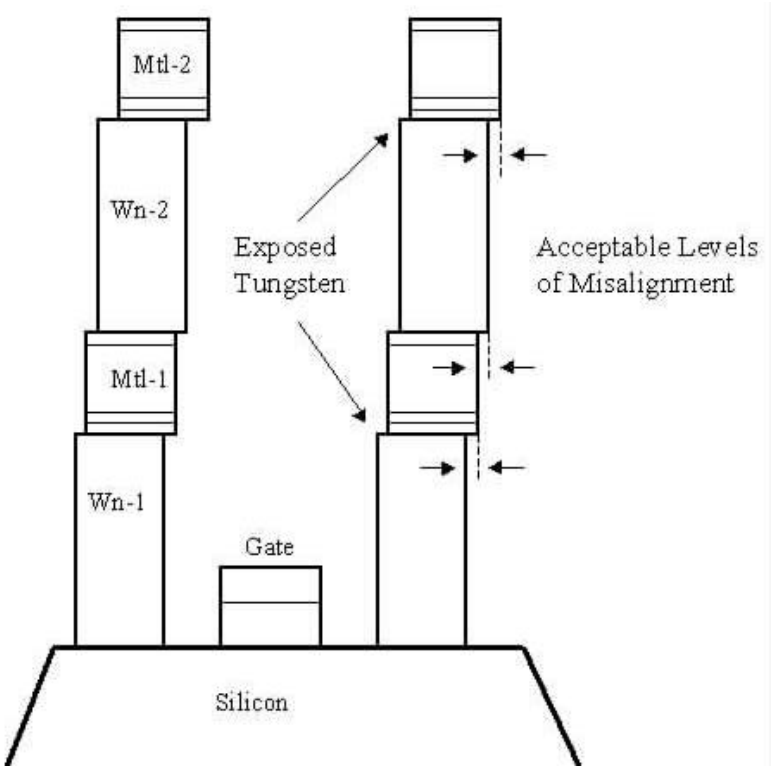

Figure 9. Allowed Misalignment in a Zero-Overlap Two Level Metal Stack

2.1.2 Mechanics of the Window Liner

To maintain performance of a scaled device the parasitic resistances of the window contacts to source, drain, and gate must be minimized. Unfortunately, contact resistance increases as contact size decreases.[vi] The foremost issue in tungsten plug integration is contact resistance especially to the P+ source/ drain. Contact resistance of tungsten plug has been strongly correlated to contact cleaning and Ti liner deposition thickness.[vii] The requirements of the Ti/TiN window liners are

- Formation of low ohmic contacts to source, drain, gate, or underlying metal.
- Barrier integrity with respect to silicon/tungsten interdiffusion
- Chemical barrier with respect to WF6 attack to silicon, titanium, or aluminum
- Uniform nucleation and adhesion of CVD tungsten[viii]
- SEM interactions with the underlying oxide, silicon, or metal surface prior to liner deposition that alters the liner in any way could compromise any of the above requirements.

As the window aspect ratios (calculated as the ratio of window depth to window diameter) steadily increase due to technology requirements, sidewall and bottom coverage of the liner decrease as a fraction of Ti/Tin deposited on the surface. Bottom coverage is defined as the ratio of the thickness of the thinnest material present at the bottom of the contact holed divided by the nominal thickness of the material deposited on the top of the dielectric. Sidewall Coverage is defined as the ratio of the thickness of the thinnest material present at the sidewall of the contact hole divided by the nominal thickness deposited on the top of the dielectric.[ix]

One study, data shown in Figure 10, found bottom coverage for a window with aspect ratio of 3:1 was only ~10%, for a standard sputter deposited film.[x]

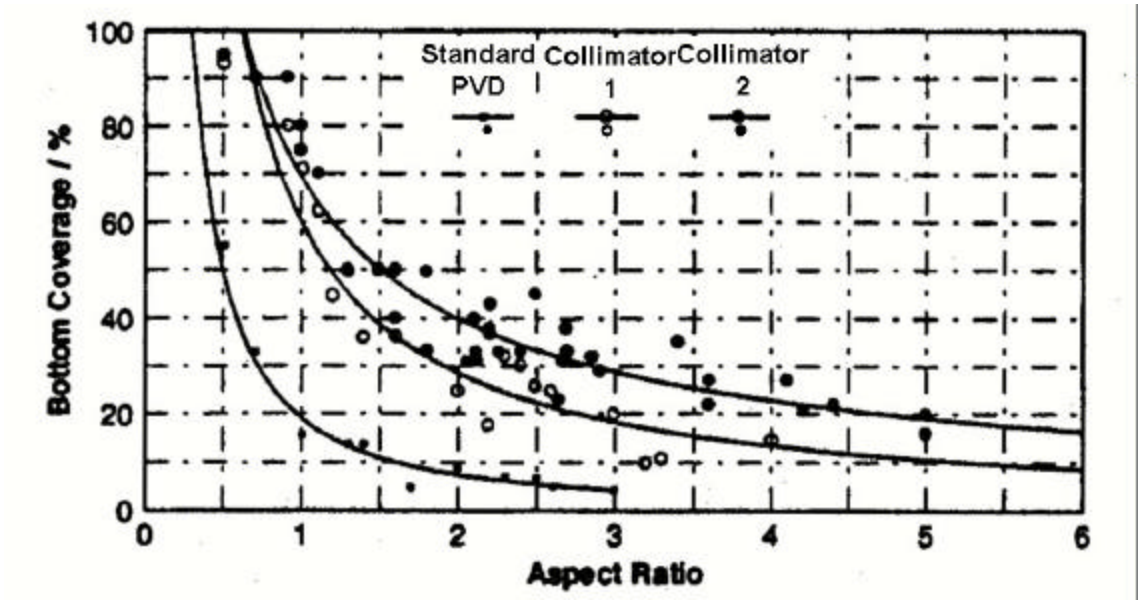

Figure 10. Bottom Coverage an Percent as a Function Of The Window Aspect Ratio for a Standard Sputtered Liner and Two Different Collimated Liners[x]

Figure 10 also shows bottom coverage for a collimated PVD liner. This is one method developed to improved conformal deposition of the liner. Collimating the sputtered atoms by placing an array of collimating tubes just above the wafer, between

the anode and cathode, to restrict the depositing flux to normal ±5°, improves bottom coverage (BC) and sidewall coverage(SC).[ix] In that study, collimating improved the bottom coverage from 10% for an aspect ratio of 3:1 to 20% to 40%, depending on the collimator used. This study also demonstrated that sidewall coverage, even for the collimated liner process, is worse than bottom coverage, in this case by approximately 33% for the window with aspect ratio of 3:1. See Figure 11.

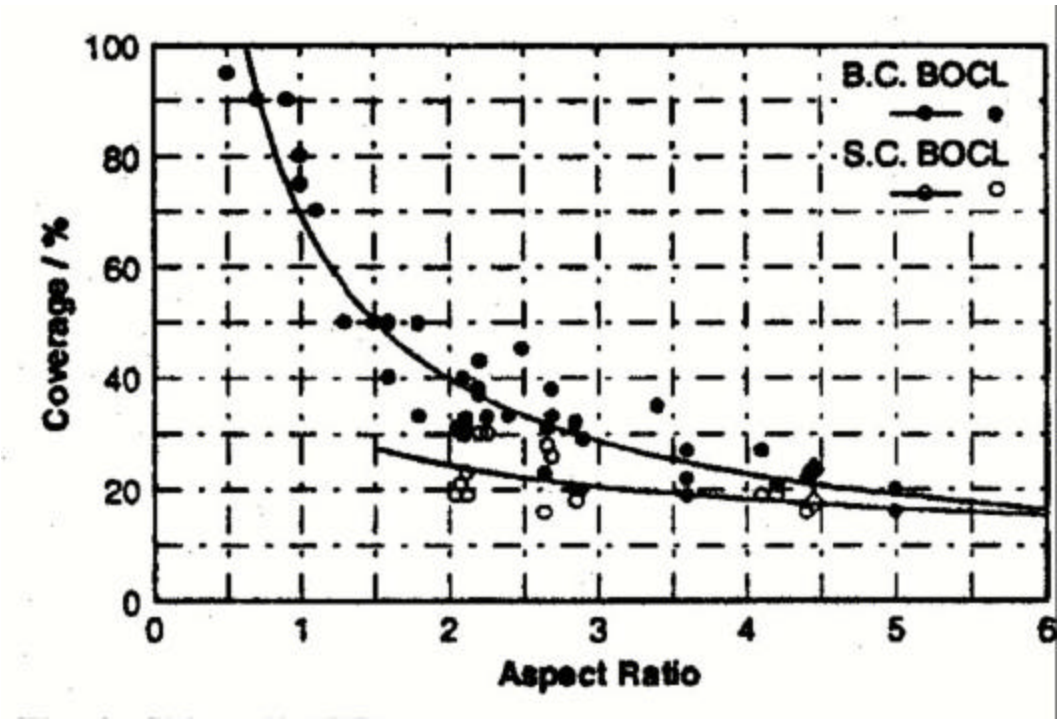

Figure 11. Bottom Coverage in Percent as a function of the window aspect ratio[x]

Two more methods for improved step coverage of the liner are currently employed. The first is CVD of the Ti/Tin liner. One study proposed the thermal deposition of TiN from a Tetrakis Dimethylamino Titanium (TDMAT) precursor, followed by an in-situ H2-N2 plasma treatment of the as-deposited film, described by following equation

$$Ti[N(CH_3)_2]_4 \rightarrow TiN(C,H) + HN(CH_3)_2$$ [xi] (1)

The second method is an ionized metal plasma (IMP) vapor deposition of the liner. This method ionizes the titanium molecules sputtering off the target and then imparts directionality to those ionized molecules. The IMP chamber is optimized to increase the number of collisions the sputtered titanium has with energetic electrons in the plasma. The non-ionized atoms and molecules deposit as in standard PVD. The ionized atoms and molecules accelerate toward the wafer surface due to the formation of a negative DC voltage at the wafer surface in an RF plasma. The acceleration of the ionized titanium reduces the angle of impingement: in essence collimating using an electrical field.[ix] IMP vapor deposition has proven to be a very effective method of depositing continuous Ti/TiN liners for windows with aspect ratios approaching 6:1. IMP Ti/TiN is the window liner used in this study to line windows with aspect ratios of approximately 4:1. IMP adds another factor to be considered, in that the impinging ions have a field associated with them that could interact with any injected field imposed by the SEM.

2.1.3 Mechanics of CVD Tungsten

Because of the conformal nature of chemical vapor deposition, CVD tungsten with WF_6 proves to be an excellent method for filling high aspect ratio windows. In addition, tungsten is an excellent diffusion barrier between aluminum and silicon. The H_2 - WF_6 chemistry provides exceptional step coverage at moderate deposition rates. The nucleation of tungsten on TiN by H_2 reduction has been shown to require substantial initiation times (up to 10 minutes). The reason for this is not clear, however, a short silane (SiH_4) reduction step has been shown to reduce the nucleation time sufficiently for production use.[xii] The silane also protects underlying Ti/TiN liner from WF_6 attack.

Once the tungsten film is fully nucleated, the tungsten deposition can be continued by H_2 reduction of WF6,[xiii] according to the following

$$3H_2 + WF_6 \rightarrow W + 6HF \quad (2)$$

$$3SiH_4 + 2\,WF_6 \rightarrow 2W + 3SiF_4 + 6H_2 \quad (3)$$

Reaction (3) is in conflict with thermodynamic predictions since the H_2 product will normally react with WF_6 according to equation (2). Experimentally however, (3) has shown to be correct implying that the silane chemistry proceeds far from equilibrium, kinetically blocking reaction (2).[xii] The kinetics of the reaction are still unclear. One study found that for all examined process conditions, silane mass transfer was the rate-limiting step, reporting that the deposition rate is first order in silane and zeroth order in WF_6 (see Figure 12 and Figure 13).[xiv]

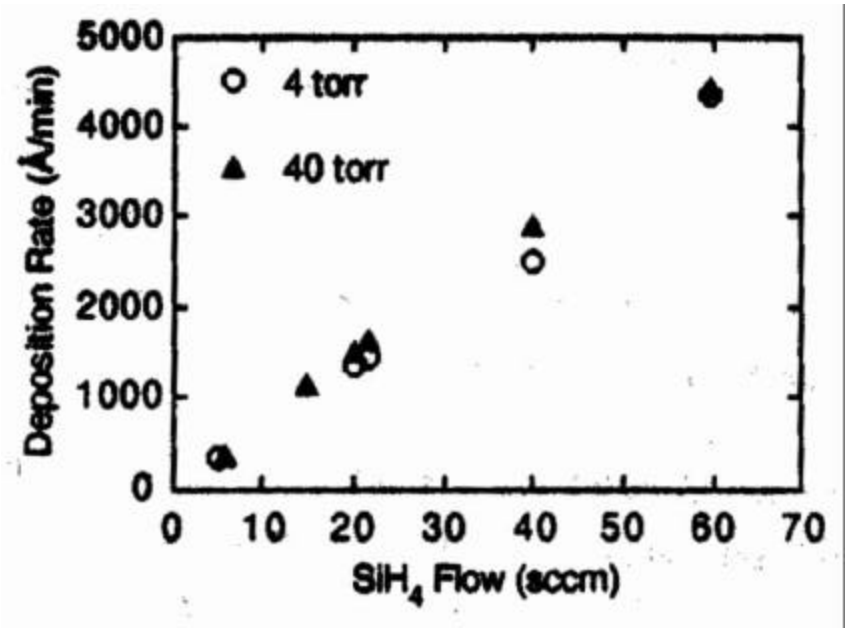

Figure 12. Tungsten Deposition Rate as a Function of Silane Flow Rate. T=440°C, SiH_4=30 sccm, WF_6=50sccm[xiv]

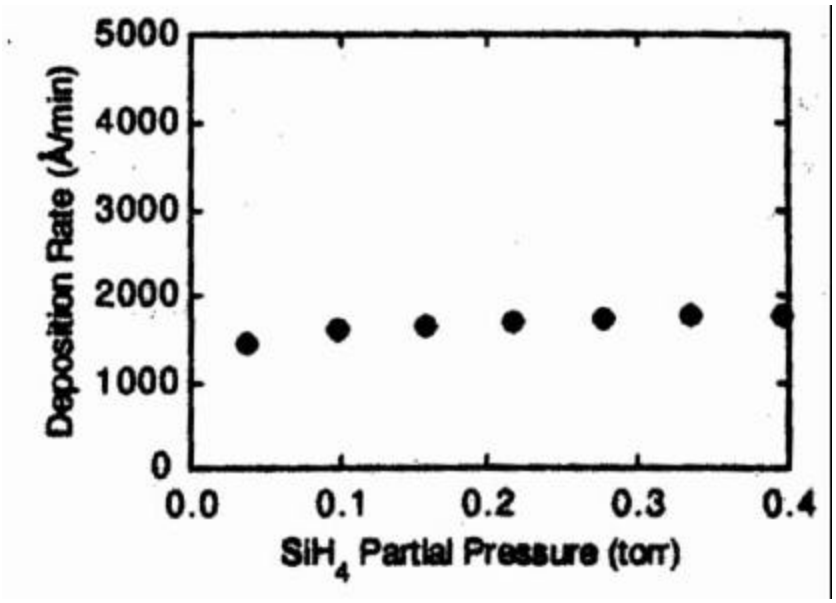

Figure 13. Deposition Rate as a Functions of Silane Partial Pressure. T=400°C, P=4-40 torr, SiH_4=25 sccm, WF_6=50sccm[xiv]

There is a processing regime where it is possible to deposit tungsten with 100% step coverage: the tungsten growth rate on the bottom and sidewall of the window equals the growth rate on the wafer surface. This results in a seam down the center of the plug, as sidewall faces grow toward each other. For a straight-walled window, and a CVD deposition that does not have 100% step coverage, the window opening pinches off before the plug is entirely filled, leaving a void down the center of the plug.[xiixii] This can be seen in Figure 14.[ix] Tungsten-CMP polishes back revealing this seam, exposing the core to the proceeding cleans.

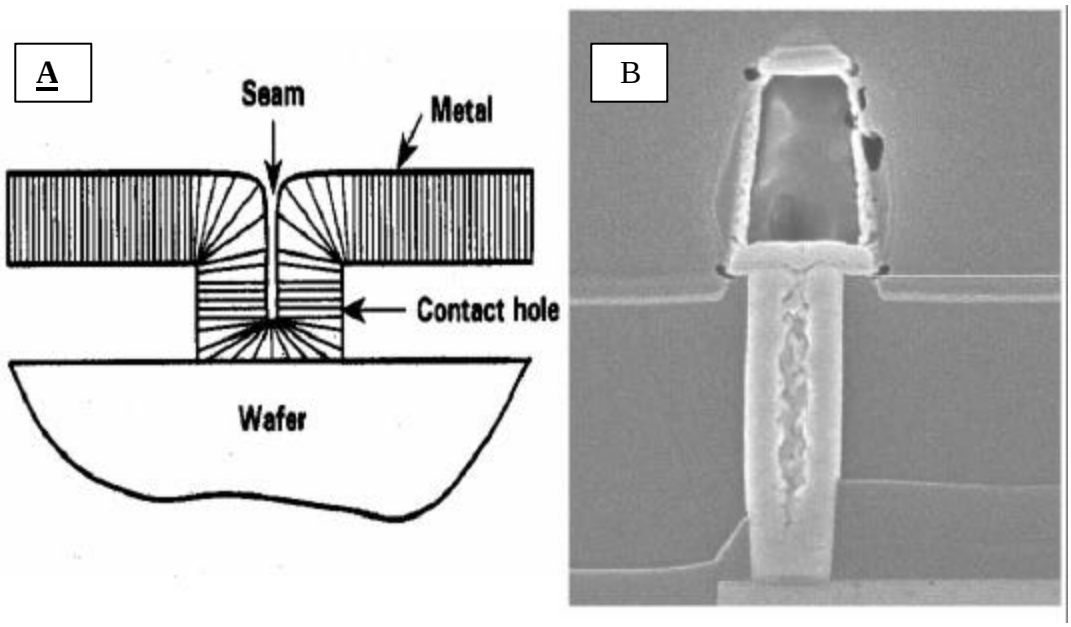

Figure 14. Center Seam of a CVD Grown Tungsten Plug Due to Growth Morphology (A) 100% Step Coverage and (B) <100% Step coverage and Pinch Off

2.1.3 Mechanics of PVD Metal Stack Deposition

Oxide and tungsten CMP leave a planar surface on which to deposit the metal levels. Therefore, a standard sputter deposition of the stack is employed. The stack consists of sequential deposition of ~200Å titanium adhesion layer, ~200Å titanium nitride barrier layer, ~5000Å aluminum 0.5% copper, and ~100Å titanium/ ~500Å titanium nitride anti-reflective coating/etch stop. The metal is then etched in a chlorine based plasma in which the principal etch product is $AlCl_3$.

2.1.4 Nature of Cleans

Up to 20% of all process steps relate to cleaning the wafer, in effort to remove particles, organic residues, inorganic residues, unwanted oxides, metallic ions, and even bacteria. A rule of thumb is that particle size must be a fifth to a tenth smaller than the

minimum feature size. Contamination can cause device failure, device performance issues, or of greatest concern, device reliability issues.[1]

As particle sizes decrease the difficulty in removing them increases. This is due to the van der Waals force and the capillary force. Solutions are formulated to minimize electrostatic attraction by altering the zeta potential. Zeta potential arises from a charge zone around particles balanced by an oppositely charge zone in the cleaning liquid, and is manipulated by varying pH, velocity, electrolyte concentration, and presence of surfactants in the solution. If the surface of the wafer can be caused to have the same polarity as the particle, the repulsive forces will keep the particle in solution.[1] Capillary forces are also important in the engineering of cleans, since these forces can be greater than van der Waals forcs[1]. Capillary forces are overcome by the use of surfactants and mechanical means such as ultrasonic scrubbing and brush scrubbing.[1] Brush scrubbing consists of rotating brushes near the wafer surface, hydroplaning across the surface rather than making contact, transferring momentum to the water being sprayed on the surface at high pressure (2000-3000 psi). Ultrasonic (20-80 kHz) and megasonic scrubs (850-900kHz) use sonic waves traveling parallel to the wafer surface to create small bubbles that collapse on the surface. These collapsing bubbles produce shockwaves, known as cavitation, that impinge on the surface, dislodging particles.[ix]

Common chemicals used in wet cleaning include dilute HF, buffered HF, H_2O_2, H_2SO_4, NH_4OH, HCl, as well as many others. These cleans are always followed by a DI rinse. Whereas front-end cleaning is well characterized, back-end cleaning is not well understood or characterized. These cleanings includes

- post-window etch to remove etch byproducts from the window bottom and side wall

- post-metal etch to remove etch residues and polymers on the sides and tops of the runners
- photoresist 'edge bead' removal to clean off excess photoresist that accumulates around the edges of the wafer during spin coating
- post-caps etch to remove residual polymer and byproducts in order to facilitate metal bonding
- post oxide and tungsten CMP remove scratches, residual slurries, and contaminants[xv]

Most back-end processing strippers are organic solvent blends, consisting of a majority solvent base, and amine (or nucleophile), and additives such as corrosion inhibitors, complexing ligands, and surfactants. The materials to be removed determine the choice of clean chemistry. There are three main types of residue.

- Organic, frequently bake-hardened or plasma-hardened photoresist, or halocarbons from the etch gases
- Inorganic residues such as SiO_2 from plasma overetch, TiN from back sputtering, and metal oxides (Al_2O_3, TiO_2, etc.)
- Mixed organic-inorganic residues such as polymer covered metal oxides/ nitrides, SiO2-covered metal oxides, or intimate mixtures of polymer and inorganic residues

The stripper formulations used for back-end cleans frequently include corrosion inhibitors, which protect the exposed aluminum at the bottom of the window or on the metal sidewall. Commonly used corrosion inhibitors include 8-hydroxyquinoline, catechol (1,2 dihydrobenzene), and galic acid. These corrosion inhibitors adsorb onto the exposed metal surface, passivating the exposed metal. This adsorbed material is then, ideally, washed away during the DI rinse. In some instances, the inhibitors form stable complexes with the exposed metal, which may not be rinsed out.[xv]

Three back-end cleans are being considered in this study. They are Ashland® ACT® NE111 (NE111), J.T.Baker® ALEG™ 310 (ALEG), and DSP+ which is manufactured by Kanto Corporation. NE111 is a buffered, pH stable fluoride-containing stripper suitable for metal and window applications. NE111 contains a corrosion

inhibitor formulated for removal of highly oxidized etch residues while reducing surface metal contamination.[xvi] Figure 15 shows SEMs of a metal stack before and after NE111 clean, in which etch residue has been removed from the metal stack

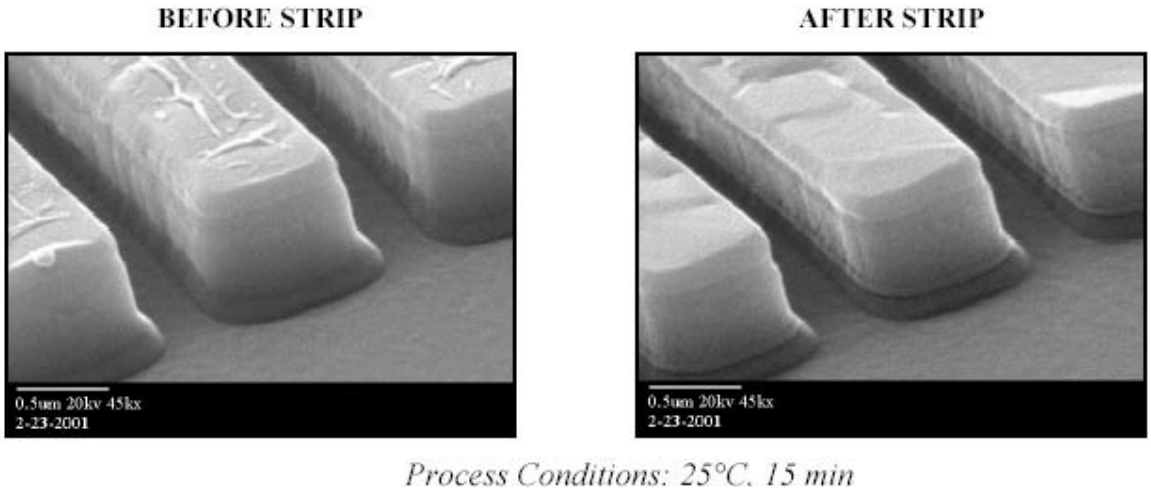

Figure 15. Product Literature Images for NE111, Metal SEMs Before and After Clean[xvi]

ALEG is a stable alkaline organic solvent blend optimized to remove both organic and inorganic materials without attacking the metal. ALEG has a pH of ~11. ALEG contains an aprotic (neither accepts nor donates protons) solvent amine system that works by dissolution. The solvent molecules penetrate, swell and dissolve organic polymers from the wafer surface.[xvii]. Figure 16 shows SEMs of a metal stack before and after ALEG cleaning. DSP+ stands for Dilute Sulfuric acid/hydrogen Peroxide. Both the sulfuric acid and the hydrogen peroxides are at a concentration of less than 10%. The (+) indicates the addition of hydrofluoric acid at a concentration on the order of parts per million. The pH of DSP+ is less than 1.[xviii] Figure 17 shows SEMs of a metal stack before and after DSP+ cleaning.

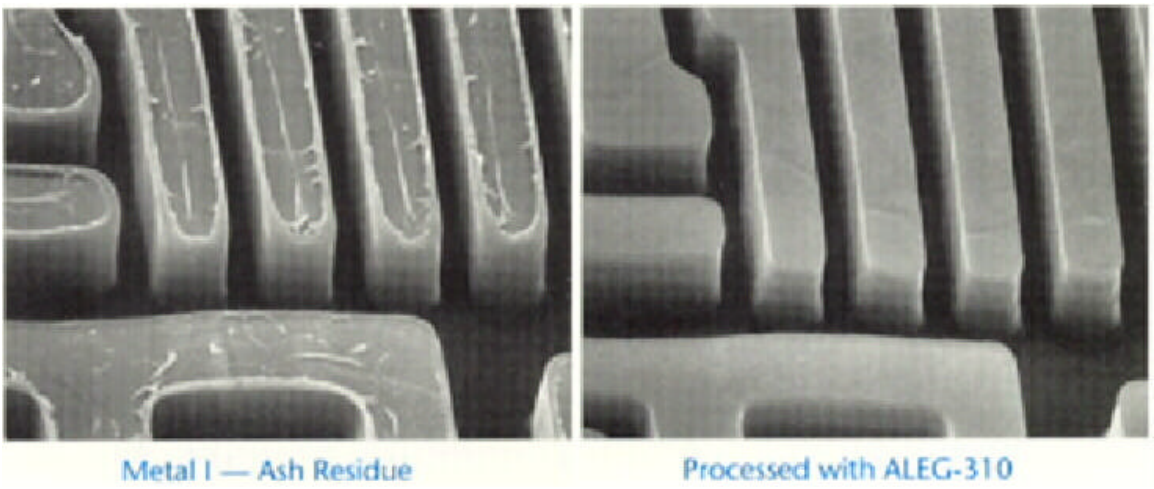

Figure 16. Product Literature Images for ALEG™ 310, Metal SEMs Before and After Clean[xvii]

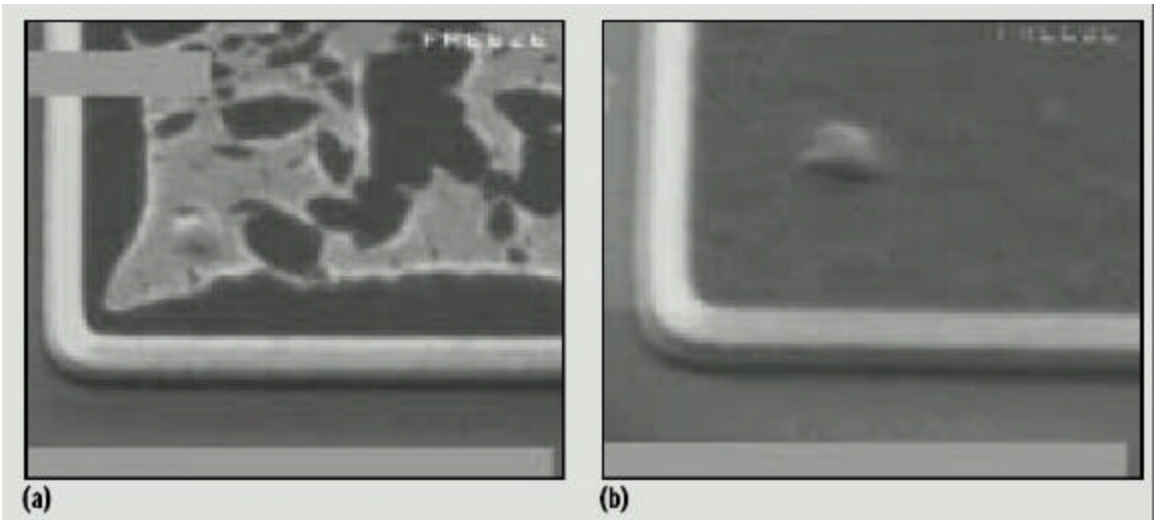

Figure 17. Product Literature Images for DSP+ of a Metal Structure (a) Before and (b) After Cleaning With the DSP Mixture[xviii]

2.2. Review of Process Induced Corrosion Literature

2.2.1Titanium Corrosion

Corrosion of the metals has been reported in numerous papers detailing both corrosion of titanium and corrosion of tungsten. Kwon et al. reported via failure in borderless tungsten plugs due to fluorine attack of the via titanium liner during CVD tungsten deposition.[xix] In this study transmission electron microscope (TEM) cross-sections found an interfacial compound between the underlying Ti/Tin aluminum capping layer and the Ti/Tin window liner. Two experimental models were hypothesized to explain the failure. The first speculated that the interfacial compound was associated with polymer residue remaining after via etching. The second speculated that fluorine attacked the titanium barrier layer during tungsten deposition due to poor barrier property of the protective TiN layer. Cleaning experiments established that via etch residue was not the mechanism. Several experiments were performed to improve the window liner, including increasing the TiN thickness, NH_3 plasma treatment of the liner, and Ti-skip barriers. All treatments were demonstrated to be effective in improving the contact resistance, confirming fluorine attack as the mechanism for failure.

Koh et al. reported corrosion of the titanium glue layer in a Ti/Tin/Al(Cu)/Tin metal stack during post metal etching polymer stripping in an alkaline (pH ~11) chemical stripper.[xx] In this study, corrosion induced window failure only occurred when the underlying tungsten plug was exposed, due to misalignment of the overlying metal. Figure 18 illustrates this liner attack.

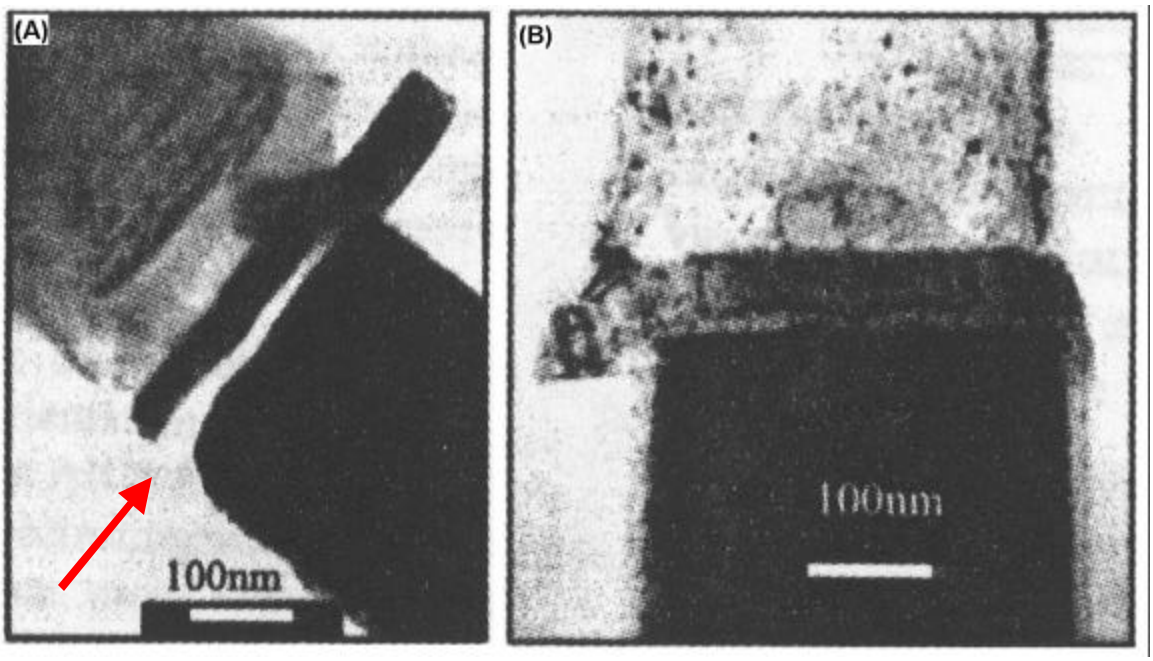

Figure 18 TEM Cross-Section Micrographs of Metal to Window Interface for (A) Zero Overlap With Ti-Liner Attack and (B) Positive Overlap With No Ti-Liner Attack[xx]

The 200Å thick Ti layer above the exposed tungsten plug is corroded, whereas the Ti-layer is not undercut when the overlying metal stack covers the plug. The corrosion is, therefore not due to a simple reaction between Ti and the stripper, rather the reaction is coupled with the tungsten underneath. In addition, when the overlying metal stack was deposited without titanium in the glue layer, no attack of the barrier occurred under the same alignment conditions, demonstrating that titanium attack was the cause of the high resistance. Furthermore, it was demonstrated that the titanium deposition method had no bearing on the titanium corrosion. A thirty second nitrogen plasma prior to the wet clean was effective in preventing attack, attributable to the formation of a thin titanium-nitride on the sidewall. An alternative stripper with a pH of about 5, was also tested, and proved to preserve the liner.

The phenomenon appeared unrelated to the electrochemical corrosion accelerated by the collection of charges on the metal sidewall during metal plasma etching. The mechanism appeared to be due to a strictly electrogalvanic reaction. Consulting the Pourbaix diagram of Figure 19 the titanium should be passivated in an alkaline solution

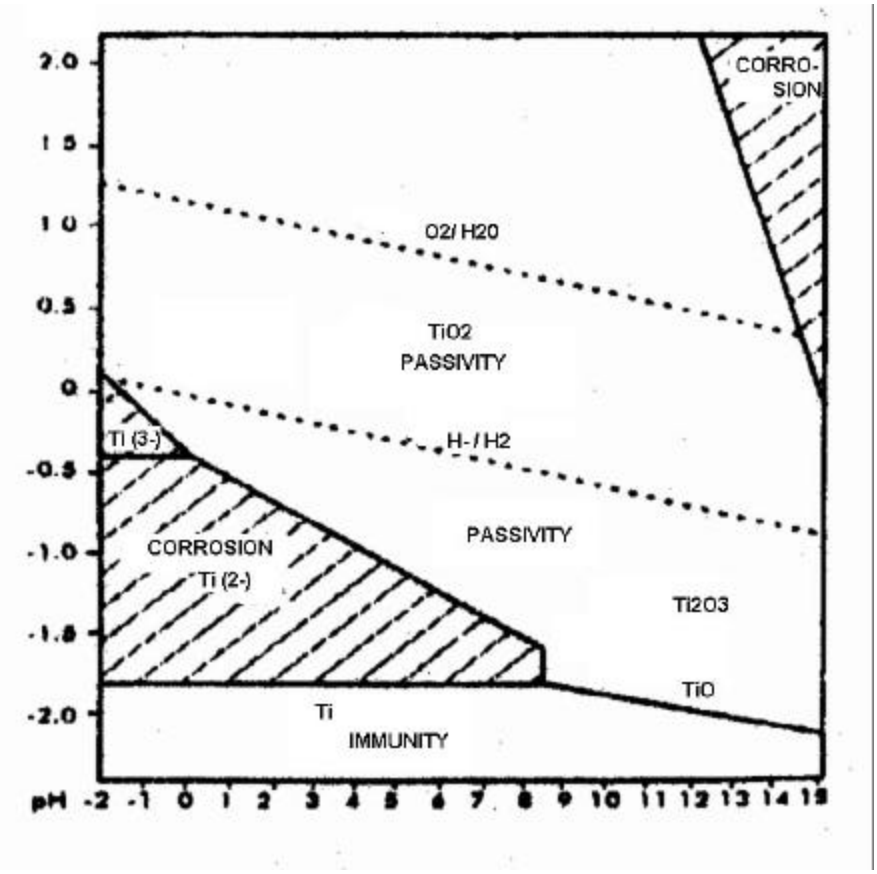

Figure 19 Potential – pH Diagram for Titanium[xx]

Titanium corrodes only at low pH in solutions without oxidizers. Therefore, the dissimilarity of metals in the electrochemical series was suggested to be the cause of the attack of titanium, since it only corroded in the presence of exposed tungsten. The oxidation of reactive titanium occurs at the anode whereby the generated electrons

(together with Ti^{2+} cations) leave the anode and flow into the alkaline stripper, which is considered an active electrolyte. This proposal established a strong correlation to the observation that coupling of titanium to the more noble metal tungsten in a reducing environment would enhance the removal of the unpassivated Ti glue layer. The reactions at electrodes in solution were proposed to be;

$$\text{Anode: } Ti \rightarrow Ti^{2+} + 2e^- \quad (6)$$

And the cathode would be tungsten where the following reaction takes place:

$$O_2 + 2(H_2O) + 4e^- \rightarrow 4(0H)^- \quad (7)$$

$$\text{Redox: } 2Ti + O_2 + 2H2O \rightarrow 2Ti^{2+} + 4(OH)^- \quad (8)$$

The solution offered in this study was substituting an alternate acidic polymer stripper which was an inactive electrolyte for the galvanic reaction between the Ti-layer and tungsten layer.[xx]

2.2.2 Tungsten Corrosion

Corrosion of tungsten in a CMOS processing technology was first reported by Bothra, Sur, and Liang.[v] In this study certain tungsten plugs were found to be etched or cored out after a post-metal solvent clean was performed on the wafers. The pH for this solvent ranged between 10-12. Prior to the clean, the windows were completely filled. The windows affected had a zero overlying metal overlap with some degree of misalignment that exposed the tungsten (Figure 20.)

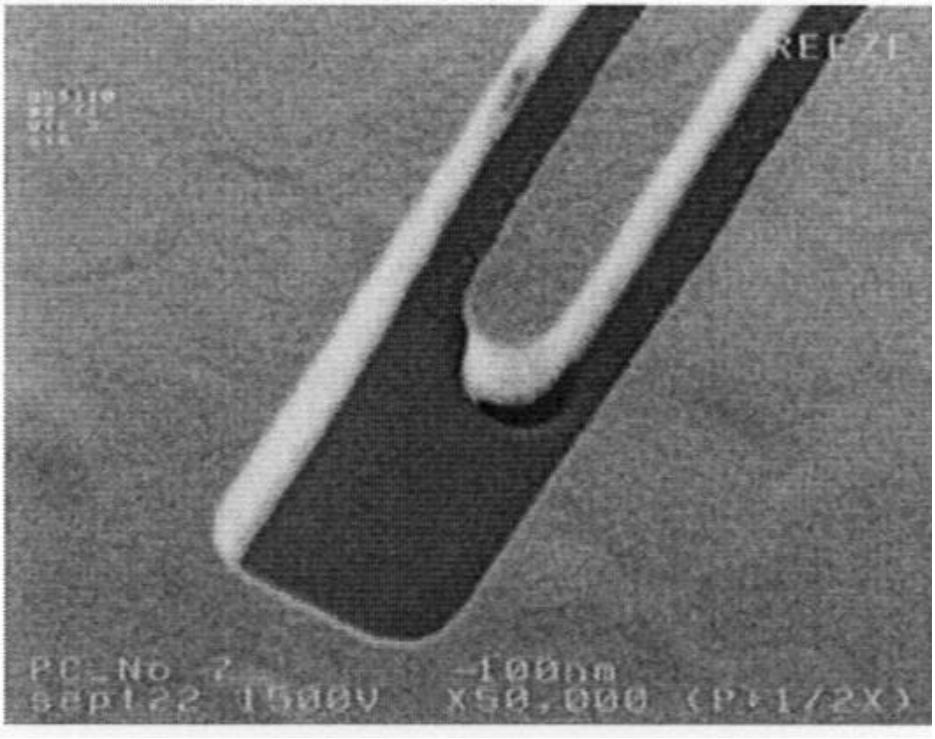

Figure 20. Top Down SEM of Misaligned Metal with Exposed Window Showing Missing Tungsten[v]

However, not all exposed windows were corroded or cored out. It was determined that the test structures were electrically charged during the metal plasma etch process. The charge then resulted in electrochemical corrosion of the exposed tungsten plugs during the subsequent solvent strip. It was discovered that a sufficient lower metal area was required to store an adequate amount of charge, while a sufficient top metal area/ perimeter was needed for charge collection during the metal etch process. An example of this can be seen in Figure 21 where columns of exposed tungsten vias are landing alternately on metal and oxide, and only the metal-landed vias exhibit coring out of the tungsten plug.

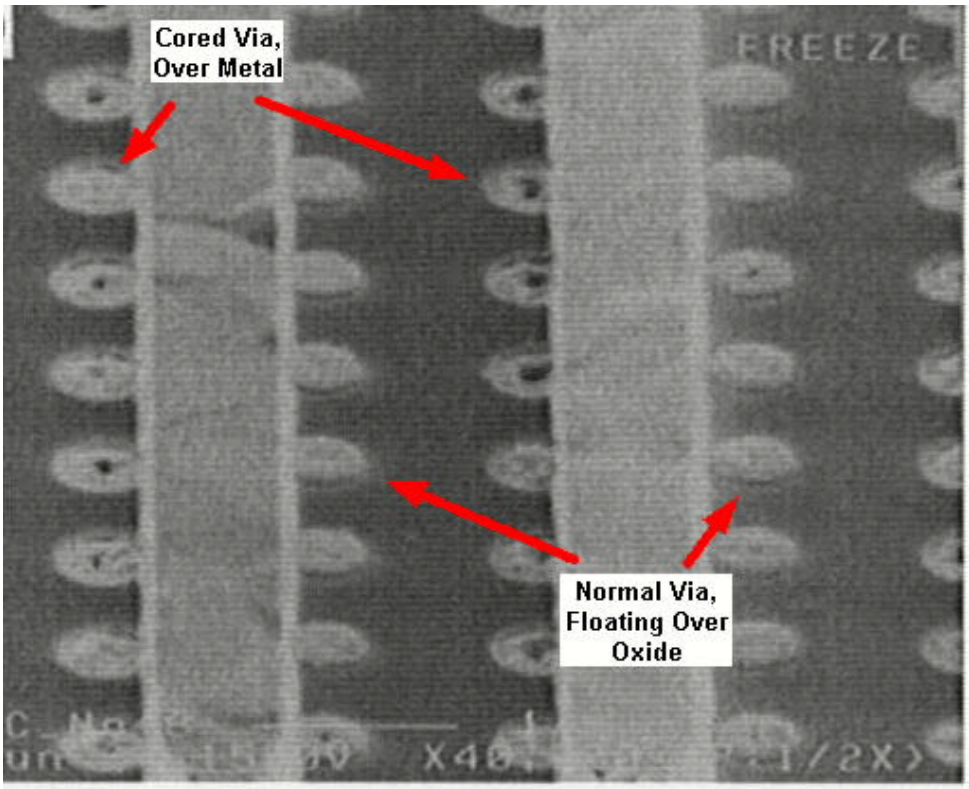

Figure 21. Columns of Exposed Vias Alternately Landing on Metal and Oxide, Showing 'Coring' of the Metal Landed Vias"[v]

The photoresist on top of metal is negatively charged by impacting electrons. The wafer itself is usually at a negative potential-the positive ions are thus accelerated across the plasma sheath potential. The negatively charged resist alters the straight path of the ions in the vicinity of the etched metal sidewall, attracting a net positive species towards the metal sidewall and providing a source of positive charge. Metal lines connected to the substrate are grounded and the charge is drained to the substrate and chuck. Floating metal structures acquire a net positive charge and float up to the plasma potential. The total capacitance of the structure is dominated by the lower metal area as it is in closer proximity to the substrate. Therefore, structures with larger underlying metal area collect a larger amount of charge. Structures with larger overlying metal perimeters collect

charge at a greater rate. The positive potential (or anodic polarization) on the test structures drives the electrochemical oxidation of the Al and W plug (the anode) according to the Pourbaix diagrams for tungsten and aluminum (Figure 22).

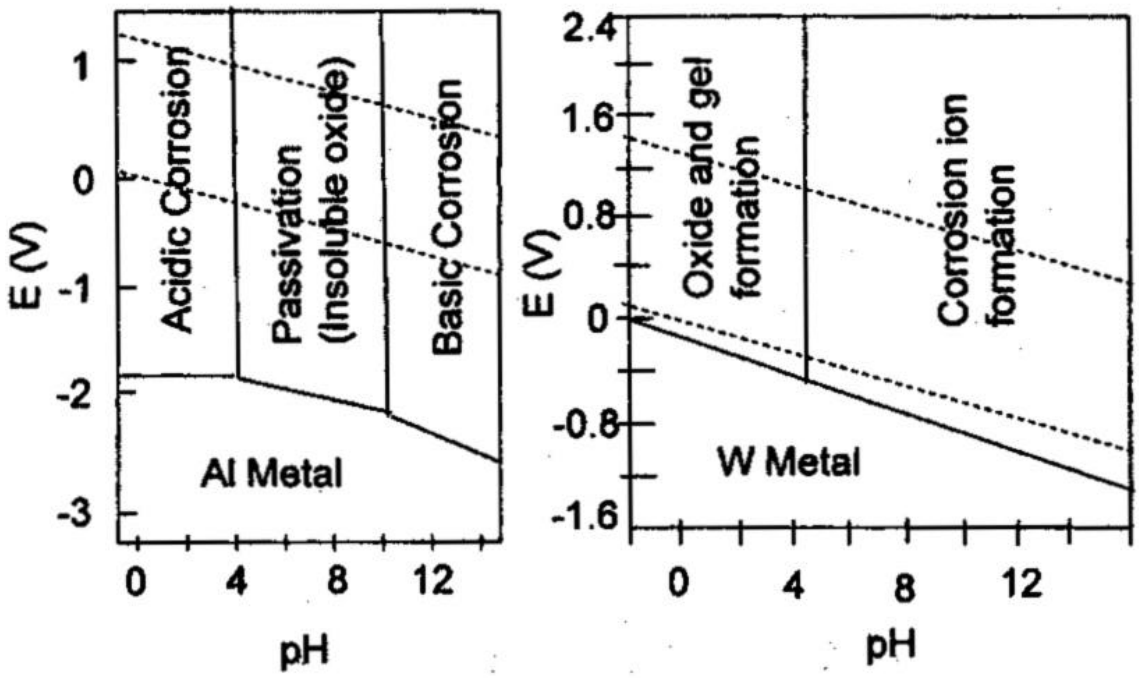

Figure 22. Pourbaix diagrams for Aluminum and Tungsten.[v]

This results in the ionization of the W atoms at the W-plug solvent interface and Al atoms at the Al-interconnect solvent interface. The metal ions thus produced react to form hydrated metal ions or metal-ion complexes. Dissolution of the metal occurs in three different states of the metal; the active, the passive, and the transpassive states as shown in Figure 23.

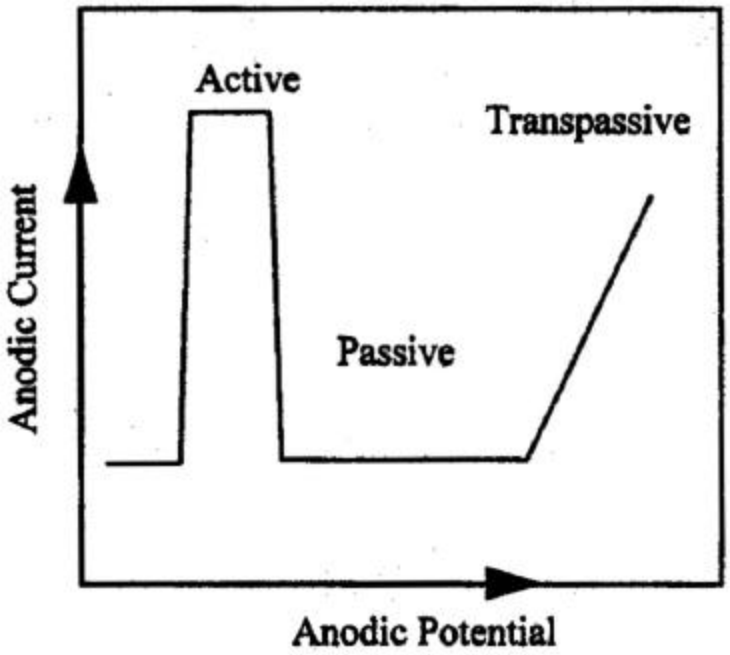

Figure 23. Three States of Metal Corrosion. (Current is Proportional to Dissolution rate)[v]

In the active state, the metal dissolution takes place at the metal surface, at a rate independent of the potential, producing an etched surface. In the passive state, the dissolution rate is extremely small and metal surface is coated with a passivating oxide. In the transpassive region the dissolution rate is finite and dependent on the potential. The dissolution normally takes place in the presence of a surface oxide film. In this study, the solvent strip chemistries used for post metal etch had a pH of 10. The tungsten dissolution mechanism was proposed as follows.

$$W(s) + 4(OH)^- \rightarrow WO_2(s) + 4e^- + 2(H_2O) \quad (9)$$

$$WO_2(s) + OH^- \rightarrow .. WO_3H(s) + e^- \quad (10)$$

(10) is deemed to be the rate determining step. At pH values above 8, the passive oxide dissolution rate increases as the WO_3 films rapidly dissolve away in alkaline solvents.[v]

The above work was confirmed by Muranaka, Kanno and Sasai.[xxi] This study found that replacing the alkaline remover with a neutral chemical prevented tungsten plug corrosion on a single window misaligned floating test structure. The post-metal etch clean with a pH of ~12 consistently corroded exposed tungsten plugs, whereas a resist remover treatment with pH of ~8.2 preserved the exposed plug

Lee et al. considered corrosion of windows connected to N+ source/drains (NSD), P+ source/drains (PSD) and gate contacts. This study investigated tungsten corrosion for exposed plugs under zero overlap metals, which were tied either to NSD and PSD, or tied to gate. It was found that, during the post-metal etch wet cleans, plugs electrically connected to the source/drains were vigorously corroded, whereas the plugs terminating at gate did not show corrosion. It was theorized that the positive charge accumulated during metal etch, was collected in the PSD-to-Ntub capacitor, whereas the capacitance of small area gate structures could not carry enough charge to drive the electrochemical corrosion.[xxii]

Hsia et al. observed galvanic corrosion of misaligned single via structures that was highly dependent on the type of electrolyte used in the post-metal etch wet-strip as well as the 'electrode' surface treatment.[xxiii] Metal etch and post-metal etch cleaning were processed using a DI water rinse and spin dry steps followed by amine based solvent chemical strips. pHs ranging from 4.5 to 11, and solutions of varying composition were studied. Characteristic AlCu corrosion pits were noticed on samples processed with chemicals having a pH value greater than 7. It was observed that, in addition to the electrochemical driven corrosion as predicted by the Pourbaix diagram, the types of electrolytes, the nature of the metal film stacks, and surface passivation also

played very important roles in the corrosion. A hydroxyl-amine based clean with pH of 4.7 corroded the tungsten plug, but an amide based solution with pH of 4.5 did not. For wafers processed with amidoxime, pH range ~8, no tungsten attack could be found on the misaligned Kelvin structure; however, the ARC-Ti layer was corroded and lifting of the TiN layer was observed. It suggests that a possible AlCu/Ti or W/Ti galvanic corrosion has occurred in which Ti reacts as an anode. A cleans solution with a pH of ~8, but containing a tertiary amine as the solvent attacked neither the tungsten nor the Ti-layer. However, a large reduction in electrical linewidth was seen, while the physical linewidth remained unchanged. It was believed that an $Al(OH)_3$ film formed according to the potential-pH equilibrium diagram of Al, which in turn consumed the zero valence aluminum in the solvent thus leading to electrical linewidth reduction. In addition, when an amine rooted chemical was replaced with NH_4F not only was no corrosion of the misaligned tungsten structures observed, but also no aluminum attack was observed either. This is attributed to a thin oxide film, which formed during the strip process in NH_4F solvent. A post-metal N_2 plasma treatment showed a drastic reduction in via resistance: demonstrating that nitridation of the metal lines passivates all metal sidewall surfaces thus diminishing the effect of Galvanic corrosion on any layer of metal in the stack.

2.2.3 Fundamentals of Corrosion

Metal corrosion occurs according to general anodic oxidation of the form

$$yM + xH_2O \rightarrow M_YO_X + aH_2\uparrow + bH^+ + be^- \qquad (11)$$

Where a + b = x. Anodic oxidation is accompanied by an equivalent cathodic reaction, usually including the reduction of H_2O or O_2.

$$2H_2O + 2e^- \rightarrow H_2\uparrow + 2(OH)^- \quad (12)$$

$$O_2 + 2H_2O + 4e^- \rightarrow 4(OH)^- \quad (13)$$

Charge transfer in the form of electrons is required for these reactions to proceed to the right, and preventing the charge transfer by minimizing current flow between the anode and cathode is, therefore an important consideration in corrosion prevention for semiconductor processing. Furthermore these equations show that the creation of H^+ ions leads to a more acidic environment near the anode while the creation of $(OH)^-$ leads to a more basic environment near the cathode. This self-generated local pH change strongly influences the corrosion behavior of metals. Pourbaix diagrams define the thermodynamically possible reactions for a metal exposed to moisture under a variety of electric potential and solution pH conditions, the regions of anodic dissolution, passivity, and corrosion. Semiconductor junctions are also a source of built in potential. This potential across the junction will be transmitted to any metal interconnects that contact the junction. Because of this, corrosion of integrated circuit metallization in the absence of metal precipitates can and sometimes do occur while the circuits are being fabricated. At high pH, many metals and their oxides and hydroxides chemically react with $(OH)^-$ to form soluble salts.[xxiv]

Regarding tungsten, its domain of stability, as a base metal, lies completely below that of water. The stability of tungstate ion is greatest in basic medium. A six-electron stoichiometry has been observed

$$W + 8(OH)^- \rightarrow WO_4^{2-}(aq) + 6e^- + 4H_2O \quad (14)$$

The proposed mechanism, fitting the observed data, consists of six steps, four of which are electrochemical in nature.[xxv]

$$W(s) + 2(OH)^- \rightarrow WO^+(s) + 3e^- + H_2O \quad (15)$$

$$WO^+(s) + 2(OH)^- \rightarrow WO_2(s) + e^- + H_2O \quad (16)$$

$$WO_2(s) + (OH)^- \rightarrow WO_3H(s) + e^- \quad \text{(RDS)} \quad (17)$$

$$WO_3H(s) + OH^- \rightarrow WO_3(s) + e^- + H_2O \quad \text{(fast)} \quad (18)$$

$$WO_3(s) + (OH)^- \rightarrow HWO_4^-(aq) \quad (19)$$

$$HWO_4^-(aq) + (OH)^- \rightarrow WO_4^{2-}(aq) + H_2O \quad (20)$$

The electrochemical oxidation of tungsten metal in basic solution proceeds smoothly to tungstate ion over a large range of current densities and hydroxide ion activities.[xxv]

As seen in the Pourbaix diagram of Figure 24, tungsten has a slight tendency to dissolve as tungstic ions WO_4^{2-}, in basic solution, decomposing water with the evolution of hydrogen.[xxvi] In the presence of non-complexing acid solutions, it tends to become covered with WO_2, W_2O_5, or WO_3, and hardly corrodes. Only the complexing acids HF, H_3PO_4 and oxalic attack it

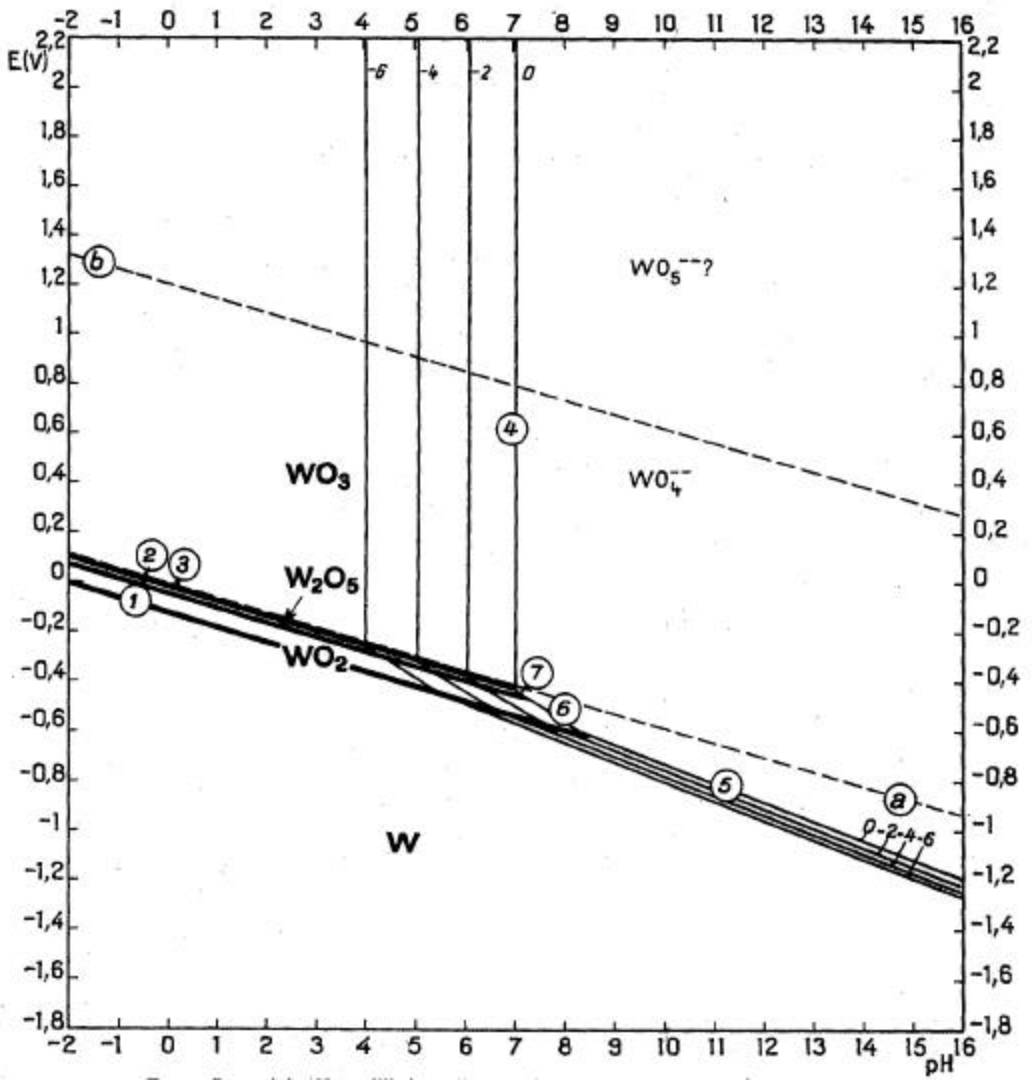

Figure 24. Potential-pH equilibrium diagram for the tungsten-water system, at 25°C[xxvi]

The hexavalent state is dissolved by anodic polarization in alkaline solutions of KOH and NaOH; however, in these solutions it becomes passive at high current densities (800 to 1750 mA/cm^2). The anodic passivation in solutions of NaOH and Na_2CO_3 is due to the formation of lower oxides which, for potentials above 60V, are oxidized to WO_3, emitting light. WO_3 and WO_4^{2-} are stable in the presence of water but are insoluble in acids, except HF with which it complexes. As pH exceeds 4.8, WO3 dissolves in water according to the reaction.

$$WO_3 + H_2O \rightarrow WO_4^{2-}(aq) + 2H^+ \quad (21)$$

Forming one WO_4^{2-} ion for two H^+ ions.[xxvi]

2.3. Scanning Electron Microscopy

As stated previously, SEM inspection is rapidly replacing optical in-line inspection for yield learning, not only because the number of defects that go undetected optically increase as critical dimensions decrease, but also because there are defects that are undetectable optically. Examples of these are open contacts due to underetch, interfacial films, line opens, and gate oxide leakages. One estimate claims that 20% or more of all defects are not optically detectable.[xxvii]

The voltage contrast phenomenon is due to electronic interactions between the impinging primary electron beam and the scan surface. The incident beam, upon impinging the surface, undergoes both elastic and inelastic scattering, which restricts the depth of penetration into the solid. Elastic scattering causes the electrons to diverge from their original path, leading to a diffusion of the primary electrons in the solid surface, with no loss in energy. Inelastic scattering causes a reduction in the primary electron energy or momentum until the solid eventually captures the electron. The region over which the incident beam interacts with the sample is known as the interaction volume.[xxviii] This interaction volume has been modeled using Monte Carlo Simulations as well as imaged directly using electron activated photoresist. Examples of the latter can be seen in Figure 25, revealing a rather pear shaped interaction volume.

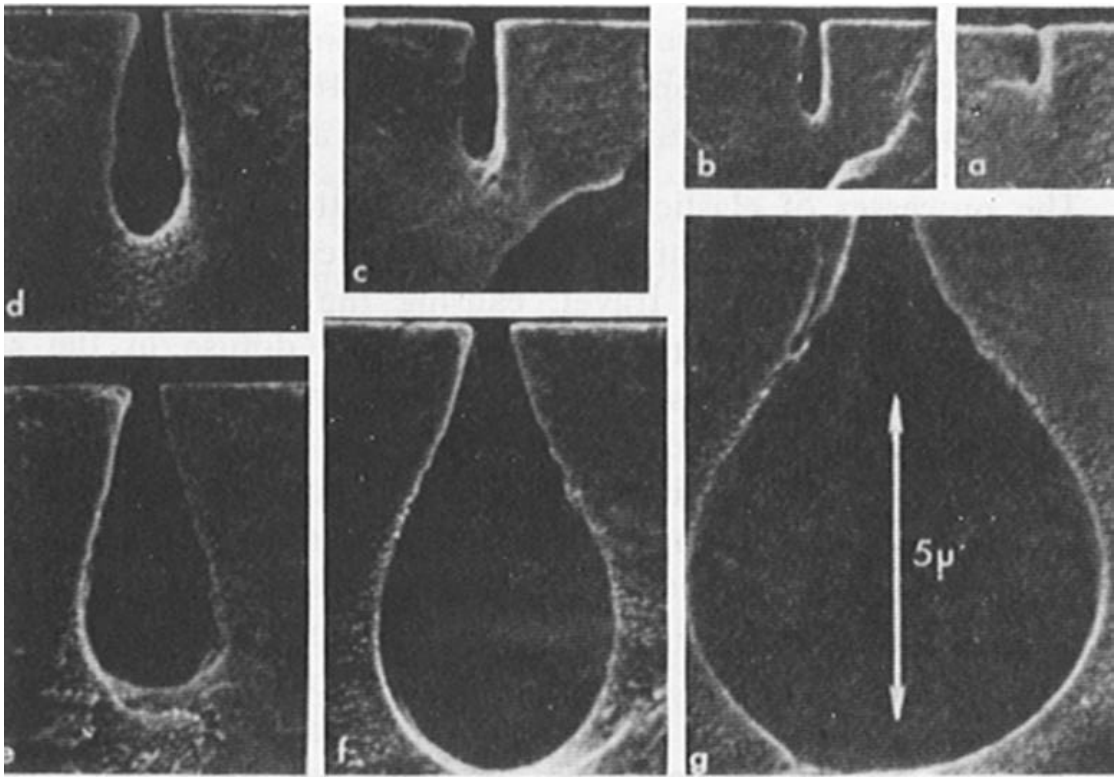

Figure 25. Electron Interaction Volume Visualization in polymethylmethacrylate. Fixed Ip and Vacc, Progressively Increasing Etch Times (a through g) [xxviii]

Monte Carlo experiments verify the pear shape for low density, low atomic number targets. As the atomic number of the target increases the pear shape transitions to a more spherical shape truncated by the plane of the surface. Figure 26 demonstrates this transition from carbon at atomic number 6 to uranium at 92. In this study, the sample surface consists of thin films ranging from nitrogen at atomic number 7 to tungsten at 74.

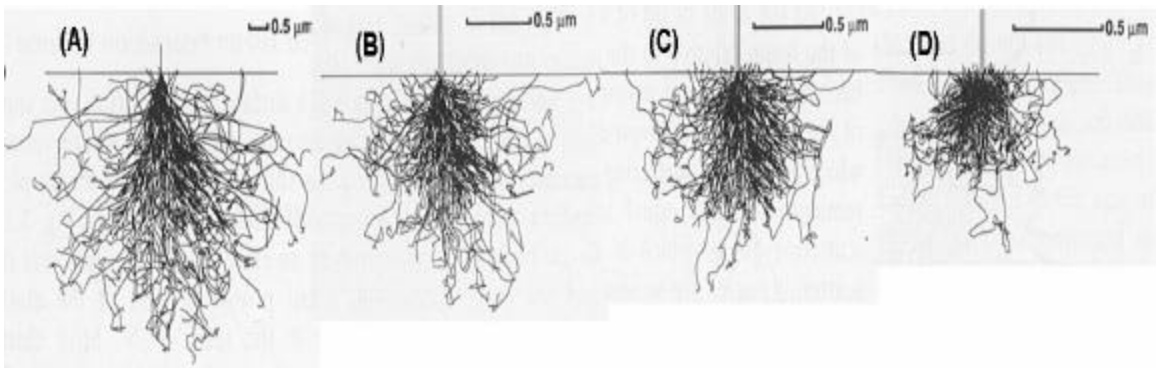

Figure 26. Monte Carlo Electron Trajectory Calculations of Interaction Volume for (A) Carbon, (B) Iron, (C) Silver, and (D) Uranium

The shape of the interaction volume does not change with changes in acceleration voltage (beam energy.) On the other hand, the size of the interaction volume is related to the incident energy. The elastic scattering cross-section is inversely dependent on the square of the energy, and the inelastic scattering is inversely proportion to the energy. Therefore, as the acceleration voltage increases the electrons penetrate the sample with greater energy and lose it at a lower rate.[xxviii] This is seen in Figure 27 of Monte Carlo calculations for interaction volume in iron with varying incident energy.

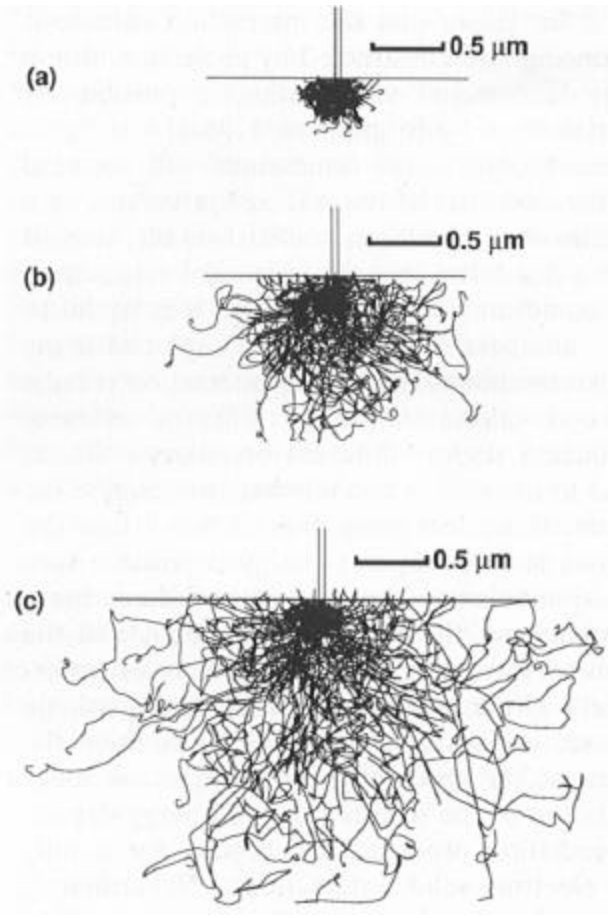

Figure 27. Electron Trajectory Monte Carlo Simulation of Interaction Volume in Iron for Vacc of (1) 10keV, (b) 20keV, (c)30keV[xxviii]

As beam energy decreases below 5keV the range (total distance the primary electron travels in the target while losing all its energy) initially decreases with linear slope. However, as the electron energy continues to decrease, the energy falls below the critical value of certain interaction processes and the range tends toward a constant value. Joy and Luo have calculated ranges for copper and gold of approximately 0.01-0.02µm for incident energies between 200ev and 1000eV.[xxix] For lighter elements these ranges will be greater.

Figure 28 gives the energy spectrum of electrons escaping from a surface being scanned by SEM. The three types of electrons described are back-scattered electrons, auger electrons and secondary electrons.

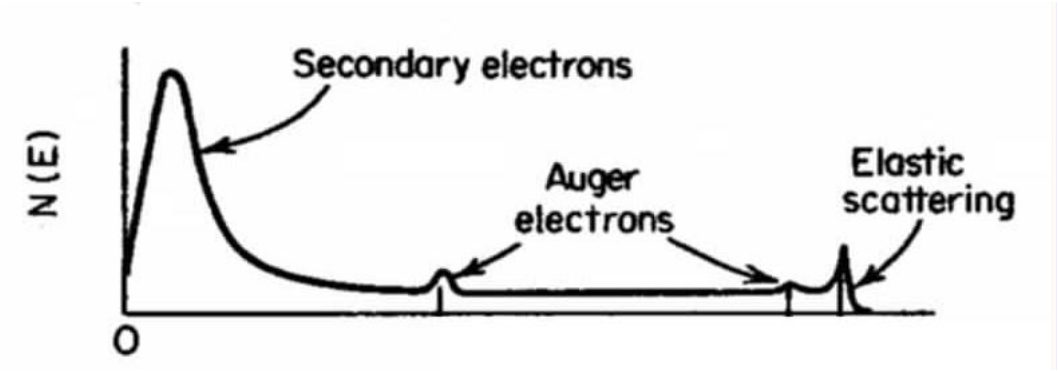

Figure 28. Electron Energy Spectrum Emitted from Surface Bombarded by Electron Beam[xxx]

The higher energy emitted electrons are the primary electrons that have been elastically scattered back to the surface. These backscattered electrons still contain most of their incident energy. The auger electrons are ejected with energies characteristic of the elements from which they were ejected, and range in value from 0 to 2400eV. The lower energy electrons ranging from 0 to 50eV and with a sharp peak around 5eV, are the result

of inelastic collisions with the primary electrons.[xxx] The ratio of backscattered electrons escaping the surface to the number of incident electrons impinging on the surface is given by the backscatter coefficient, ?.

$$? = n_{BSE} / n_I = I_{BSE} / I_I \quad (4)$$

Where n_{BSE} is number of backscattered electrons and n_I is the number of incident electrons, expressed in current I_{BSE} is the backscattered current and I_I is the incident current. ? is dependent on atomic number and varies from < 0.10 for the lightest elements, up to ~0.50 for the heaviest. The ratio of secondary electrons escaping the surface to the number of incident electrons impinging on the surface is given by the secondary electron coefficient, d.

$$d = n_{SE} / n_I = I_{SE} / I_I \quad (5)$$

where n_{SE} is the number of secondary electrons and n_I is the number of incident electrons, expressed in current I_{SE} is the backscattered current and I_I is the incident current. d is relatively insensitive to atomic number and the energy distribution of the emitted secondaries is a narrow peak centered at ~5eV with 90% having less than 10eV.[xxviii]

Since the escape depth of secondaries is extremely shallow (a few nanometers), the number of incident electrons generally exceeds the number of emitted electrons, that is, (? + d) is less than one. However, as the primary beam energy is reduced below 3keV, the primary range becomes so shallow that the number of secondaries with enough energy to escape the surface rapidly increases and (? + d) can exceed unity. This is especially the case for dielectrics, where the ratio can reach as high as 20. A plot of (? +

d) can be seen in Figure 29. The point E_2 is the crossover point, where the total number of incident electrons equals the total number of ejected electrons.

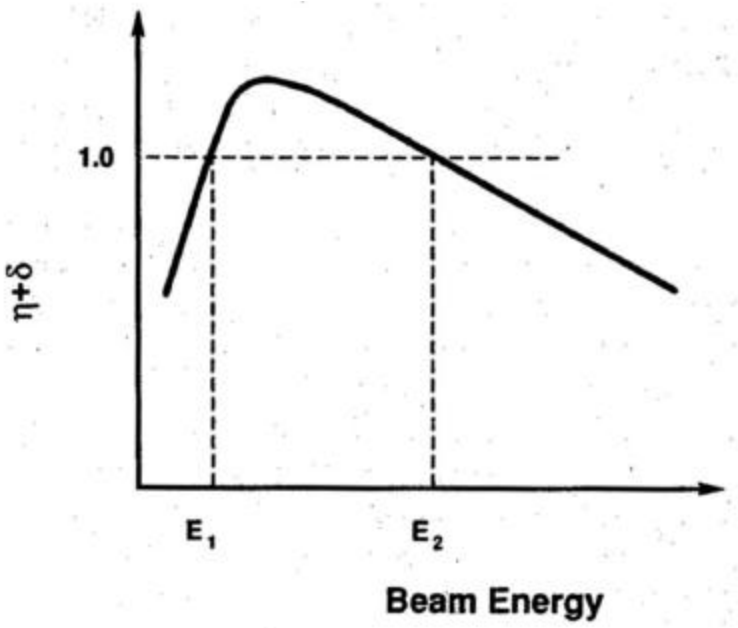

Figure 29. Total Emitted Electron Coefficient as a Function of Beam Energy[xxviii]

If the sample being scanned is a grounded conductor, electrons can be readily supplied or carried away and the (? + d) ratio will remain constant over time as the surface is being scanned. If, however, the sample is not grounded a steady state (? + d) ratio greater or less than unity is not possible. In the case of beam energy greater than E_2, electrons will be injected into the surface and the surface will develop a negative potential. This negative potential will increase to the point where the surface voltage will eventually match the acceleration voltage and the incident electrons are deflected away from the specimen. This is a complex unstable phenomenon, with a changing state of surface potential due to the accumulation and discharge of electrons. In the case of beam energy less than E_2, more electrons are emitted than are incident, and a net positive potential will

develop on the surface of the specimen. This net positive potential will act to increase the incident energy of the primary electrons, in essence increasing the acceleration voltage. The effective beam energy will increase, and the (? + d) ratio will decrease toward unity, as described in Figure 29. Simultaneously, the increasing surface potential will capture secondary electrons escaping the surface, effectively lowering the (? + d) curve. Eventually (? + d) will reach unity, and a steady state will be achieved on the surface of the specimen, where the number of primary electrons equals the number of secondary and backscattered electrons. A constant surface voltage will be attained that will be less than the delta between Vacc and E_2, and most likely on the order of the 5-10eV characteristic of the secondary electron energy. The value for E_2 is material dependent. E_2 values have been reported for glass passivation and quartz of 2.0keV and 3.0keV respectively.[xxviii]

For specimens that are non-grounded conductors, the surface charge accumulation will eventually bleed away once the beam is turned off. The same can not be stated for insulators. Charge clouds accumulate at the surface producing intense irregular local fields, which can be great enough to result in breakdown of the gate oxide in MOS devices. Within a thin surface layer as deep as 2keV a certain mechanism of two-dimensional charge conduction functions to relax charge accumulation. The thickness of the surface layer is no less than the escape depth of the secondaries (2 to 50nm). Beyond this thin surface layer, primary electrons that are driven deep into the dielectric layer produce a fixed irreversible charge accumulation embedded in the dielectric.[xxxi] It is possible that this embedded charge will generate a field at the oxide surface, which could then locally disturb subsequent processing steps.

A final phenomenon particular to SEM inspection is contamination by foreign substances. Generally considered to be hydrocarbon deposition, the effect observed is a 'scan square', which can be quite severe. The source of the hydrocarbon is thought to be the sample itself since modern vacuum systems have very efficient traps for volatiles. It appears that the hydrocarbons are attracted to the scanned surface, migrating along the specimen surface.[xxviii] Figure 30 is an SEM image of a 'burn' mark caused by an in-line CD-SEM.

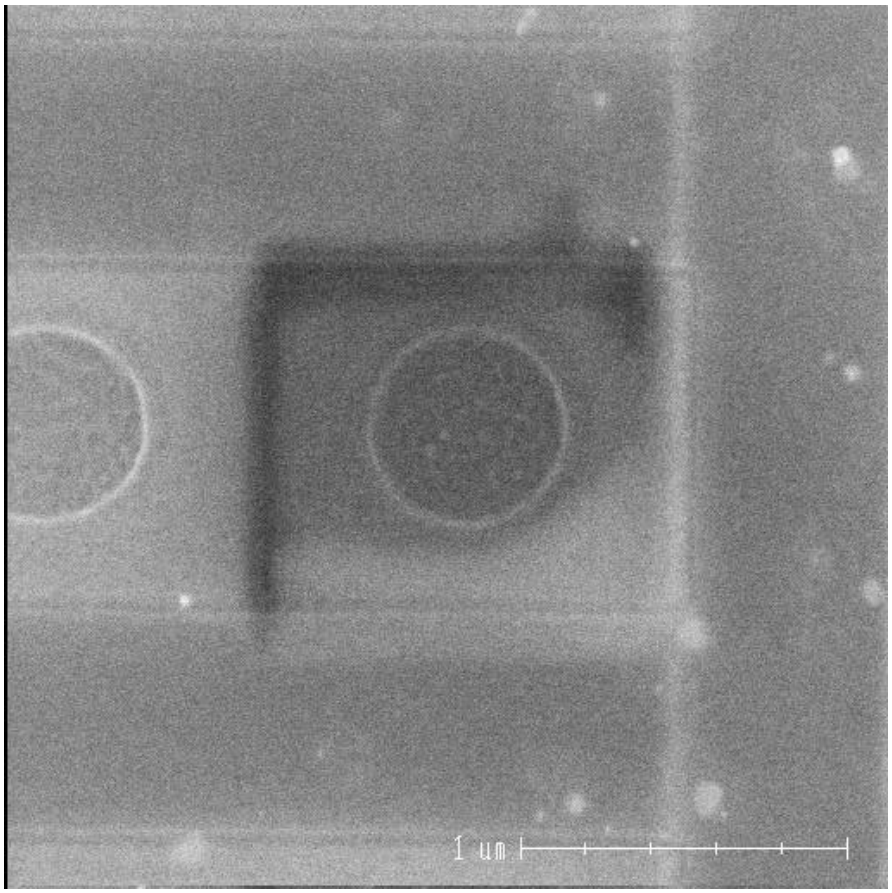

Figure 30: SEM Image of Hydrocarbon 'Burn' Mark Caused By In-Line CD-SEM

This carbon 'burn' mark can become an interfacial film that could disrupt the electrical characteristic of the sample involved.

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