ATOMIC SCALE ENGINEERING OF DIELECTRICS ON SILICON CARBIDE

• VANDERBILT UNIVERSITY

• AUBURN UNIVERSITY

• OAK RIDGE NATIONAL LABORATORY

• OVERVIEW OF THE PROGRAM

  – Leonard C. Feldman

  • Dep’t. of Physics and Astronomy
    • Vanderbilt University

  • Solid State Division
  • Oak Ridge National Laboratory
POWER DEVICES

• POWER RECTIFIERS
• BIPOLAR TRANSISTORS
• POWER THYRISTORS
• POWER MOSFETS
• INSULATED GATE BIPOLAR TRANSISTORS
• MOS-GATED THYRISTORS
POWER MOSFETS

- The performance of a power device is ultimately limited by the power dissipation, $P_D$, within its structure:
  - $P_D = I^2 R_{on}$

- For many MOSFET type devices this condition can be expressed in the ideal case in terms of the (ideal) specific on-resistance, which is to be minimized:
  - $R_{on-sp} = \frac{4BV^2}{\epsilon_s E_c^3 \mu_n}$.

- The denominator is Baliga’s figure of merit and is a factor of 200 greater for silicon carbide than silicon.
For a typical DMOSFET the on-resistance is given by:

\[ R_{on} = R_{N^+} + R_{CH} + R_A + R_J + R_D + R_S \]

In the ideal case \( R_D (R_{bulk}) \) dominates.

In the real case \( R_{CH} (R_{surf}) \) makes a significant contribution, even in silicon.

This will be more severe in SiC, with its relatively poor interface characteristics.
POWER MOSFETS

- Applying the figure of merit, $R_D$ may become small and $R_{on}$ may be limited by the channel contribution.

- One limiting factor preventing realization of this large improvement is the low electron inversion layer mobilities resulting from non-ideal interfaces in SiO$_2$/SiC.

- Our work is addressing this issue, and other breakdown and frequency limits imposed by imperfect dielectric/SiC interfaces.
CHANNEL RESISTANCE

- \( R_{\text{CH}} = \frac{L}{(Z \mu_{\text{ns}} C_{\text{ox}} [V_G - V_T])} \)

where:
- \( Z \) = width of the channel,
- \( L \) = length of the channel
- \( \mu_{\text{NS}} \) = the interface mobility.
On-Resistance of 23 mΩ-cm² is realistic for 600 V 4H-SiC UMOSFET

Pitch = 10 μm
μ_{Bulk} = 400 cm²/Vs
μ_{Inv} = 50 cm²/Vs
E_{4+} = 1.5 MV/cm
E_{4} = 3.0 MV/cm
E_{SiC} = 1.0 MV/cm

Ω.cm²

Breakdown Voltage (V)

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I-V Curves for Thermal Oxide Based 4H-SiC UMOSFET

$R_{ON} = 162 \, \text{m}\Omega \cdot \text{cm}^2$

$T = 250^\circ \text{C}$

$\mu_{inv} = 4 \, \text{cm}^2/\text{Vs}$

$N^+ \text{ Polysilicon Gate}$

$BV = 100 \, \text{V}$

$Pitch = 29 \, \mu\text{m}$

Poor Body Contact

$V_G = 18 \, \text{V}$

$14 \, \text{V}$

$10 \, \text{V}$

$6 \, \text{V}$

$mA$

Volt

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CHANNEL MOBILITY

• Determined by:
  – Interface Roughness
  – Interface Charge
  – Impurities
  – Strain
Universal Mobility Curve

Temp = 300K

Phonon Scattering

UMC obtained from $I_{DS} - V_{GS}$ data at low $V_{DS}$

Invariant to:
- $T_{ox}$
- $V_{sb}$
- $N_{channel}$

Surface Roughness Scattering

$\begin{align*}
\text{3.3Vdd} & \quad 90A, 0.5V_T \\
\text{2.5Vdd} & \quad 65A, 0.5V_T
\end{align*}$
GOALS

• GOAL: SYSTEMATIC AND FUNDAMENTAL APPROACH TO OPTIMIZATION OF THE DIELECTRIC/SILICON CARBIDE INTERFACE WITH MODELLING AND CRITICAL CONTROL OF THE SURFACE/INTERFACE PARAMETERS.

» MODULES

• Roughness minimization, interface strain
• Interface chemistry, hydrogen, oxynitrides
• In-situ oxidation
• Electrical characterization, C-V, Mobility
• Dopant redistribution via point defect injection
• Z-contrast TEM for interface structure
• First principles and atomic scale theory
FIRST SPECIFIC GOALS OF DARPA/EPRI PROGRAM

• CHARACTERIZATION OF SURFACE ROUGHNESS, CARBON RESIDUALS
  – Bozack (AU), Holland(ORNL), Streitz(AU/Theory), Feldman(VU)

• OXYNITRIDATION, HYDROGEN PASSIVATION
  – Feldman (VU), Weller(VU), Williams(AU) Pantelides(VU/Theory)

• IN-SITU OXIDATION
  – Tin(AU), Pennycook(ORNL), Pantelides(VU/Theory), Chen(AU/Theory)

• ELECTRICAL CHARACTERIZATION
  – Williams (AU), Tin(AU), Weller (VU), Chen (AU/Theory)

• THEORY
  – Pantelides(VU), Streitz(AU), Chen(AU), Feldman (VU/EXP.)

• MOBILITY DETERMINATION
  – Williams(AU), Feldman(VU)
INTERFACE CHEMISTRY

• Interfacial chemistry has been the central element of research in the formation of high quality semiconductor/dielectric interfaces.

• Essential elements are:

  • Formation of stoichiometric dielectrics
  • Impurity incorporation for dopant control
  • Hydrogen incorporation for “dangling bond” suppression
  • Minimization of undesirable impurities at extraordinary levels
HYDROGEN AS A DEFECT PASSIVATOR

• Hydrogen creates a strong bond with unpaired electrons and is the ultimate passivator in the Si/SiO2 system.

• The control of hydrogen passivation is a delicate process resulting from a competition between two solid state chemical reactions:
  
  \[ \text{Si} + \text{H}_2 \rightarrow 2 \text{Si-H} \]
  
  \[ \text{and} \]
  
  \[ 2 \text{Si-H} \rightarrow \text{H}_2 + \text{Si} \]

• Different reaction rates and temperature dependences are expected for SiC, but control will result in substantial lowering of the interface defect density.
OXYNITRIDES FOR SiC

- Oxynitrides are known to be an effective diffusion barrier for boron in silicon processing. Therefore it is useful to explore the same materials system as a aluminum diffusion barrier in SiC processing. Al diffusion into the gate oxide is known problem in SiC device fabrication.

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SURFACE SMOOTHING

It is clear that interface state measurements will be difficult to interpret unless the issues of surface smoothing are solved. We will consider three approaches:

1) Hydrogen etching at 1650C, atmospheric pressure
   Ramanachandran et al., J. Elec. Mat. 27, 308 (1997).

2) Implantation induced softening
   Holland et al, unpublished

3) Cluster beam bombardment
   Yamada et al, Hirvonen et al.
INTERFACE STRAIN

• Interface strain at the Si/SiO$_2$ interface is attributed to the large difference in the volume content of the silicon in the oxide layer versus the bulk. The insertion of an oxygen atom between two Si atoms results in a 30% linear expansion.

• Interestingly the silicon content of the oxide is quite comparable to the Si content of SiC, suggesting the possibility of a less strained interface.
INTERFACE STRAIN CONTROL

• Strain and interface defect generation in SiO$_2$/Si is driven by:
  
  • $\rho(Si)_{\text{oxide}} \ll \rho(Si)_{\text{substrate}}$

• For SiC:
  
  • $\rho(Si)_{\text{oxide}} \equiv \rho(SiC)_{\text{substrate}}$

• With controlled non-stoichiometric growth:
  
  • $\rho(Si)_{\text{oxide}} \equiv \rho(Si_{1-x}C_{1+x})$
THIN SILICON CARBIDE

• Hydrogen induced cleaving of bulk SiC

• An extraordinarily important development on the horizon. Successful implementation of this process will allow many device layers from a single 500μm wafer. This will have a significant impact on the economics of silicon carbide.

• SiC formation on silicon

• A relatively simple process involving the high temperature reaction of propane (methane, acetylene) with silicon. This produces a reasonable SiC layer of high structural quality (but not device quality) for materials studies. In particular detailed issues of interstitial injection, normally associated with oxide formation on silicon, can be investigated for SiC oxidation.
DIVISION OF LABOR

- L.C. Feldman (Vanderbilt)
  - Surface roughness, interface control, interstitial injection, carbon residuals, interface stress, oxynitridation.

- J. Williams (Auburn)
  - In-situ oxidation, non-stoichiometric growth, interface stress, nitrogen analysis, electrical characterization and surface science of SiC.

- S. Pantelides (Vanderbilt)
  - Theory-interstitial injection, interface structure, molecular dynamics, process modeling of SiC