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EVALUATION OF RAPID THERMAL PROCESSING SYSTEMS AND THEIR ROLE IN FABRICATION OF NEXT GENERATION CMOS FABRICATION

By

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In the last decade, improvements in performance of CMOS (Complementary Metal Oxide Semiconductor) has been unprecedented. As the size of the transistor is shrinking, new developments in the fabrication processes become a necessity. To manufacture an IC, Silicon wafer goes through processes like diffusion, photoresist coating, developing, UV exposure, inspection, etch, film deposition, implant, anneal, polishing, and eventually testing. The role of rapid thermal processes is evolving to meet the demands of next generation CMOS technology. The purpose of this paper is to describe three modern RTP systems and evaluate them in terms of their process capability on control wafers, throughput, and cost of ownership.

Tool A is a RTP system equipped with wafer rotation and multiple pyrometer based temperature control system to optimize within wafer uniformity during soak and spike anneals. Tool A has 1-2 C of run to run temperature variation. Tool A also has 2-3 C of within wafer variation for soak anneals as shown by Arsenic and Boron implanted control wafers. During emissivity independence testing, Tool A showed higher sheet
resistivity values for low backside emissivity test wafers than high emissivity wafers. This shows the a temperature offset exists between high and low extremes of emissivity spectrum. This must be taken into account in creating anneal processes for production.

Emissivity independence testing for Tool A and Tool B (Ripple pyrometry based tool) shows similar results as shown by difference of about 2 ohms/square between high and low emissity wafers on soak and spike anneal processes. Tool B shows about 1-2 C and 7-9 C of within wafer temperature variation for soak and spike anneal respectively.

Tool C(Hot Liner based tool) is feasible to be used for older technologies about 0.25 um as it have wider process window for temperature control and higher within wafer uniformity. This stems from the fact that the pyrometer views the Hot Liner and deduces wafer temperature. Run to run variation for this system ranges about 5-7 C and within wafer temperature variation is about 8-10 C.

Tool A has the highest cost of ownership almost 4 times as much as of Tool B. Tool A has two and half times the throughput as of Tool B. Tool B and Tool A are similar in process capability study as shown by sheet resistivity based control wafers. Tool A has an additive advantage of detecting "bare" Silicon temperature even at low temperature region of 400-700 due to small operating wavelength of its pyrometer. Tool B's ripple pyrometer does not sense the "bare" Silicon wafer radiation until it reaches 700 C. Tool B has throughput of about 30-40 wafers per hour for standard soak anneals. Tool C is most cost effective tool but does not meet requirements for manufacturing technologies beyond 0.25 um. Its capacity is about 25 wafers/hr for soak anneals.
CHAPTER 1

INTRODUCTION

There has been an unprecedented growth of semiconductor industry after invention of bipolar and field effect transistors 30-40 years ago. Figure 1.1 shows SIA roadmap for next generation Complementary Metal Oxide Semiconductors (CMOS). This enormous growth in VLSI technology is mainly due to continued shrinking of transistors. The driving force behind this effort has been higher packing densities, higher circuit speeds, lower power dissipation, and lower cost per function.\(^{(3)}\)

The rapid advances in VLSI technology are continually being fueled by improvements in microprocessor architecture and fabrication technologies. It is the latter on which this paper focuses, particularly giving its attention to rapid thermal processes in IC fabrication.

As the size of the transistor is decreasing, critical electrical parameters and performance requirements are also changing. Some of these challenges entail short channel length, reduced supply voltage, reduced gate oxide thickness, and decreased junction depth. To fabricate devices that meet these challenges, novel materials and novel process technologies have been introduced in the processing of semiconductors. One of the process requirements for scaled device is source-drain engineering that involves formation of ultra shallow junction and sharp dopant profiles. Rapid thermal processors are toolsets that are used to activate these implanted dopants. Temperature
control and increased ramp rates in Rapid Thermal Processes (RTP) ensure minimum
diffusion of lightly doped drain region (LDD), preservation of established channel length
from lithography, and optimum drive current.

The purpose of this paper is to describe and compare three modern Rapid Thermal
Processing systems in terms of their process capability, throughput, cost of ownership,
ambient control, and temperature control mechanism. The process capability evaluation
of different RTP systems will be done in terms of within wafer uniformity, wafer to
wafer/run to run variation, backside emissivity independence testing, and repeatability
testing on standard implanted control wafers.
Figure 1.1: CMOS Roadmap: Planar CMOS Grand Challenges (2)
CHAPTER 2

REVIEW OF LITERATURE

2.1 RTP Fundamentals

The basic operational principal of RTP systems is radiation heat transfer. This is effectively achieved by lamp based heating system in which the process chamber is securely isolated to achieve optimum heating. One feature that distinguishes RTP systems from traditional diffusion furnaces is the existence of thermal inequilibrium between chamber walls, and wafer itself. It is this feature that allows “rapid” heating of wafers. Second distinction comes from temperature control devices used in both systems.

These basic features of RTP systems are shown in the Figure 2.1 schematically. This includes thermally isolated process chamber inside which cooling water lines are installed. Process chamber also contains gas inlet for the process and ambient gases used in a given process. Lamps are installed on top, bottom and sides of the chamber and also cooled by air or nitrogen based cooling. Inside the process chamber and close to the lamps, several quartz plates or tubes are installed to effectively isolate wafer from process chamber. Inside the quatzware, quartz tray is installed which contains Silicon (Si) edge guard ring and quartz pins on which wafer resides. Silicon wafer stays on three to four quartz pins surrounded by Si edge guard ring to eliminate edge to center temperature variation. Quartzware is cooled by CDA (Clean Dry Air cooling) or PN2 (Pure Nitrogen based cooling). Pyrometer assembly is mounted at the bottom of the chamber and looks
at the emitted radiation from backside of the wafer. Standard pyrometer consists of a
Photo detector that translates optical radiation to electrical signal and in turn temperature
measurement is obtained.

The basic understanding of physics of heat transfer in RTP is to recognize that it
consists of number of radiating bodies at different temperatures, each with its
characteristic energy spectrum. The lamps may be at 2000-3000 C (filament), the wafer
temperature around 25-1200 C, and the chamber walls between 20-400 C depending on
system design and wafer set temperature. (1)

**Emission of Radiation:**

The radiation emitted by hot objects has a well-defined spectral distribution. In
the simple case of black bodies, this distribution is only a function of temperature, and
given by Planck’s relation:

\[
M(\lambda, T) = \frac{\varepsilon C_1}{\lambda^5 \left( \exp \left( \frac{C_2}{\lambda T} \right) - 1 \right)}
\]

Where,
- \(M\) = Spectral Radiance
- \(C_1\) and \(C_2\) = constants
- \(\varepsilon\) = emissivity
- \(\lambda\) = wavelength
- \(T\) = Temperature

The power distribution for a black body at various temperatures are plotted in Fig.
2.2. It is apparent that as the source temperature increases, the radiant energy output at
all wavelength increases. In addition, the output at shorter wavelength increases very rapidly with temperature so that the wavelength range containing the bulk of the radiant energy shifts toward lower wavelengths at higher temperatures. \(^{(1)}\)

However, the real components of a system are not perfect black bodies. They emit less radiation at each wavelength than a black body. An approximation to the real emission behavior can be done by scaling blackbody radiation by constant factor called emissivity \(\varepsilon\). Such “real” or “grey” body has the total emitted power equals to \(\varepsilon\) times that of a black body at the same temperature, as shown in Fig. 2.3. \(^{(1)}\)

**Absorption of Radiation:**

Radiation incident on a surface is transmitted through the surface and absorbed. A black body absorbs all the radiation incident upon it. Real bodies reflect a fraction \(R\) of the radiation, and absorb a fraction \(A\). So \(A+R=1\). From thermal equilibrium principles, incident radiation \((I)\) must equal the sum of reflected \(R\) and emitted \(E\) radiation and thus \(1= R+E\) and so \(e = 1-R=A\).

An important result of this is that for all real radiation sources, average emissivity and absorptivity may not always be equal. The reason behind this is due to different spectral distributions from the emitted radiation (e.g. from Si wafer) and the incident radiation (e.g. from lamps). \(^{(1)}\)

**Thermal Conduction inside Silicon:**

Although an average temperature across Si wafer remains constant, transient temperature differences can develop across the wafer due to a different balance between
emission and absorption in different regions. Most common factors are outlined below:

- The different geometrical and radiation situations at the edge as compared with the center of a wafer.
- The different energy balances that occur in regions as a result of different film stack, overlayers, and pattern definition.

**Conversion of Absorbed Radiant Energy to Heat**

The absorbed radiation interacts with the matrix electrons which then transfer heat energy to the lattice as summarized in Fig. 2.4. This interaction is inefficient if the density of free electrons is low, and the photon energies are lower than the threshold required to excite electrons across the bandgap (wavelengths longer than one micron). The bulk absorption coefficient is then a strong function of both wavelength and temperature. \(^{(1)}\)

**Sources of Radiation:**

The significant sources of radiation in a typical system include the lamps, their reflections, the reflections of the wafer itself, chamber walls and their reflections. These are shown schematically in Fig. 2.5 and Fig. 2.6. Each of these sources has its own spectral distribution of radiant energy, given by the product of the black body curve and the spectral emissivity at each wavelength. Typical temperatures range to 6000 C (for arc lamps), 3000 C (Tungsten halogen lamps), 600-1200 C (Si wafer), and 200-400 C (quartz chamber walls). \(^{(1)}\)
The basic features of a lamp source rapid thermal anneal system, shown schematically in vertical section. A silicon wafer (seen edge-on) is held (usually on thin quartz pins) in thermal isolation inside a cell, containing a controllable gas ambient. One (or two) light sources heat the wafer through transparent window(s), aided by reflectors. A pyrometer views the wafer back through a series of windows and a filter, in order to monitor and control wafer temperature.

Figure 2.1: Basic Features of RTP System

Figure 2.2: Spectral Radiance versus Wavelength for Black Bodies
Figure 2.3: Spectral Radiance versus Wavelength for Real Bodies\(^{(1)}\)

Figure 2.4: Micro-scale Radiation Effects during RTP\(^{(1)}\)
Figure 2.5: Sources of Optical Radiation in RTP System\(^{(1)}\)

Figure 2.6: System Components affecting the Pyrometer during RTP\(^{(1)}\)
**Optical Properties of Semiconductors:**

Depending on the incident radiant energy, there are two kinds of optical absorption processes which may occur in a semiconductor. The first kind of absorption process involves the absorption of photons which have energies equal to or greater than the bandgap energy of a semiconductor. This type of optical absorption is called the fundamental or interband absorption process. The fundamental absorption process is usually accompanied by an electronic transition across the forbidden gap, and as a result excess electron-hole pairs are generated in semiconductor. The absorption coefficient due to interband transition is usually very large.\(^{(4)}\)

In UV to visible spectral range, typical values of absorption coefficient for most semiconductors range from \(10^6\) cm\(^{-1}\) near the UV wavelength to 1 cm\(^{-1}\) near the cutoff wavelength of the semiconductor (e.g., 0.4 to 1.1 um for Si). Si is direct bandgap material as shown in Fig. 2.7. Fig. 2.8 also shows relationship between absorption coefficient and photon energy for Ge at different temperatures. Figure 2.9 shows the cutoff wavelength for several semiconductors such as Silicon, and Germanium.

However, the absorption coefficient becomes very small (e.g. less than 1 cm\(^{-1}\)) when the photon energies fall below the bandgap energy of the semiconductor. This optical absorption process is called the free-carrier absorption process. The energy bandgap varies between 0.1 and 3 eV for most semiconductors, the fundamental optical absorption occurs in the visible to IR spectral regimes.
Therefore, most semiconductors are opaque from UV to IR spectral range, and become transparent in the far infrared spectral regime (ie. greater than 10 um wavelength). (4)

![Diagram of Direct and Indirect Transitions](image)

Figure 2.7: Direct and Indirect Transitions associated with the Fundamental Absorption Processes in a Semiconductor (4)
Figure 2.8: Square Root of Absorption Coefficient versus Photon Energy for Ge (4)

Square root of the absorption coefficient versus photon energy for a germanium sample with temperature as a parameter. Insets show the spectral resolution. After Macfarlane et al. (3) with permission.
Figure 2.9: Solar Spectral Radiance versus Wavelength for different Optoelectronic materials (4)
**Temperature Measurements in RTP:**

Pyrometers are the instruments of choice for in-situ temperature measurements. They enjoy the benefits of non-contact, real-time, and fast thermal response. Most limiting factors are their operating wavelengths and spatial resolution which could present severe limitations.

Standard pyrometer is housed at the bottom of the chamber. It views center of the backside of the wafer. Sophisticated control systems have two pyrometers that include one pyrometer viewing the lamps and one viewing the wafer. From the reflectivity of the backside of the wafer, emissivity can be calculated and lamps can be adjusted to compensate for different backside film types and thickness.
2.2 CMOS RTP Processes

As the size of the transistor shrinks, the total number of processing steps are significantly increasing. Scaled devices require reduced thermal budget to meet end of the line yield specifications. This has led to lesser number of diffusion and high temperature growth processes as the total thermal budget decreases. Many high temperature and deposition/growth processes (e.g. Field Oxide growth, nitride deposition, furnace based anneal) have been replaced by low temperature Plasma Enhanced Chemical Vapor Deposition (PECVD), Low Pressure Chemical Vapor Deposition (LPCVD), and Rapid Thermal Chemical Vapor Deposition (RTCVD) techniques.

RTP systems have been exploited for number of key processes for CMOS fabrication. This ranges from classical process steps such as source/drain implant anneal, barrier formation, silicidation to novel applications such as oxide growth, growth of gate dielectric, growth of heterostructure layers (e.g. SiGe heterostructure devices). Thus RTP has potential to perform implant anneal, metal silicidation, oxidation, and deposition of thin dielectric films. Figure 2.10 shows cross section of CMOS (Complementary Metal Oxide Semiconductor). Major RTP processes used in CMOS fabrication is outlined below.

**Implant Anneal Processes:**

The function of these processes is to activate dopant materials by annealing the implant damage in Si substrate. These processes can be used at tub, gate, and source/drain implant levels. Implant anneal is high temperature process requiring
temperatures from 950 C to 1050 C for standard Arsenic, boron dopant activation. As the junction depth is decreasing, anneal times are becoming smaller and smaller. For technologies below 0.25um, anneal times of 3-10 seconds have become a standard. Need for higher ramp rate and short anneal time processes referred as “spike” anneal have become greater than ever. Different implants levels are depicted in Figure 2.11 showing cross section of submicron Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

**Metal Silicidation Processes:**

This is one of the classical applications of rapid thermal processes requiring lower temperature regime of about 400-700 C for Cobalt (Co) and Titanium (Ti) silicidation. The function of this step is to form a good contact that is chemically stable and electrically reliable. Contact resistance is used to evaluate the quality of metal silicidation process. To obtain good metal contact on the active area of the device, it is critical to monitor oxygen concentration in real time during this process. State of the art RTP tools are equipped with in-situ oxygen sensor that provides real time data on oxygen concentration in the chamber. If oxygen leak exists in the chamber, metal oxide tends to form at the contact site causing poor device performance. $R_c$ (Contact Resistance) and $R_s$ (Sheet Resistivity) measurements are used as barometer for metal silicidation, and implant anneal processes respectively. Besides $R_c$ and $R_s$, number of other indirect parameters such as Ion (speed), Ileakage (leakage current), $V_t$ (Threshold voltage), and $L_{\text{effective}}$ (electrical channel length) can also be used as evaluators of these processes.
Figure 2.10: Cross-Section of CMOS (3)

Schematic device cross section for an advanced CMOS technology.
Figure 2.10: Cross-Section of CMOS

A: Isolation STI Fill
B: Low Rs Contact Leakage
C: "Dual" Metal Gate
D: CD Control
E: High Gate Dielectric
F: USJ Extension
G: Contact Junction Depth
H: Channel Doping Steep Retrograde
EVALUATION OF MODERN RTP SYSTEMS

3.1 Materials and Methods: Control Wafer Preparation

Arsenic Control Wafers:

Procedure:

Standard p-type 8" Silicon wafers were used as starting material for preparation of control wafers. These wafers were scrubbed to remove any particulates. This was followed by RCA clean using HF, NH\textsubscript{4}OH, H\textsubscript{2}O\textsubscript{2}, and H\textsubscript{2}O solutions. Then these wafers were implanted with Arsenic at 25KeV of energy and 1e16 atoms/cm\textsuperscript{2} dose.

Anneal/Test Conditions:

For soak anneal testing, anneal conditions were chosen to be 1025 °C for 20 seconds in 5% oxygen ambient. Sensitivity of Arsenic implant controls at these conditions is about 0.7 ohms/square/°C. For spike anneal testing, anneal conditions were chosen to be 1125 °C for dwell time of less than 0.7 seconds in 5% oxygen. Sensitivity of Arsenic wafers for spike anneal is about 0.5 ohms/square/°C.

Boron Control Wafers:

Procedure:

Starting material for Boron implant controls was n-type 8" Silicon wafers. This wafer were scrubbed and cleaned for particle removal. This was followed by RCA clean using HF, NH\textsubscript{4}OH, H\textsubscript{2}O\textsubscript{2}, and H\textsubscript{2}O solutions. This was followed by 200 A of screen Oxide deposition to prevent any channeling of Boron atoms. This was followed by 10KeV,
1.5e15 atoms/cm² Boron implant. This was finally followed by Oxide strip step by concentrated HF solution.

**Anneal/Test Conditions:**

Anneal conditions for Boron implanted wafers were chosen to be 950°C for 20 seconds in 100% Nitrogen ambient. Sensitivity of Boron is about 2.2 ohms/square°C.

**Emissivity Independence Testing:**

The starting material for this testing was p-type 8” Silicon wafers. These wafers were implanted using Arsenic at the same energy and dose as mentioned above. The backside of these wafers had different emissivity values ranging from 0.2-0.8. These wafers were prepared using proprietary processes.

**Sheet Resistivity Measurement:**

Sheet resistivity of control wafers were measured using RS75 Prometrix tool. This measurement was done using 121 sites with three mm of edge exclusion.

**Test Run Set Up:**

Test runs for control wafers were set up using dummy wafers as pre-heat wafers to condition the process chamber. Two dummy wafers were used to pre-heat the chamber.
3.2 Tool A: MIMO(Multiinput-multioutput system) Control System/Wafer Rotation Based RTP system

3.2.1. System Overview

This novel RTP system is characterized by multi-zone lamp heating source, multi-point temperature measurement system and real-time wafer temperature control. This tool addresses major challenges for designing robust RTP systems particularly problems such as emissivity compensation, accuracy and repeatability of wafer temperature measurement.

Multi-point temperature measurement systems have potential for providing better within wafer uniformity than traditional single point measurement. Figure 3.1 shows the design of lamp head with the process chamber. This assembly consists of gas handling, low pressure operation under load lock, and wafer handling systems. Wafers are supported in the chamber by a silicon carbide edge guard ring. This ring is mounted on a quartz cylinder which extends into the chamber bottom where it is supported by bearing. This bearing is magnetically coupled to an external motor which is used to rotate the wafer and assembly. (8)

Lamp head has characteristic design of honeycomb of tubes in a water jacket assembly. Each tube contains a reflector and a tungsten halogen lamp assembly which forms a honeycomb light pipe arrangement. (8) This close packed arrangement of light pipes provides the radiant energy sources with high power density. Wafer rotation is used to smooth lamps to lamps variations and enhance within wafer uniformity.
As shown in Figure 3.2, the lamps are arranged into twelve independently powered radial lamp zones. These lamp groups can be combined in up to six distinct radial groups for optimum temperature control. The output of the lamp is shown as uniformly shaded concentric rings since the rotation action of the wafer has the effect of averaging over the output intensity of the lamps in that group. A quartz window separates the lamp head from the chamber.

**Temperature control and measurement:**

Challenges for modern RTP system lies in optimum temperature control which is achieved by pyrometry. Areas of improvement in temperature measurement include the following: Minimizing the interference from the background radiation, minimizing the impact of wafer emissivity has on temperature, and finding an improved way of performing in-situ calibration of the pyrometer.

To accurately measure the wafer temperature, and background interference from tungsten halogen lamps especially in low temperature regime, single sided heating was employed. The pyrometers were mounted on the bottom of the chamber, opposite the light source. (8)

**In-situ emissivity measurement:**

The spectral radiance from the wafer depends on the temperature and the spectral emissivity. A strategy that is employed here is to create “virtual black body” by forming an optical cavity between the chamber bottom and wafer backside. Ideally, where the reflectivity of the cavity is unity, wafer backside acts as a perfect “black-body” having emissivity value of a unity.
A highly reflective coating is applied to the bottom of the chamber. This feature greatly reduces the dependence of temperature measurement on wafer emissivity. To eliminate residual temperature variation due to variation in backside emissivity, a second probe is mounted near the first probe. The wafer emissivity readings from these two probes can be used to find an actual wafer temperature. (8)

3.2.2. Results and Discussion

Process capability of Tool A was evaluated in terms of its performance of implanted control wafers. Several types of control wafers were used as described in section 3.1. Figures 3.6 to 3.11 outlines this tool's performance.

**Soak Anneal Performance:**

Soak anneals are high temperature (950-1050 C) process with longer (about 10-20 seconds) anneal times. This study included wafer to wafer and run to run repeatability testing, within wafer uniformity performance, low temperature metal silicidation testing, and emissivity independence testing using wafer with different backside.

The repeatability testing was done mainly by measuring sheet resistivity of implanted Arsenic and Boron wafers. Test runs were arranged with dummy preheat wafers followed by actual sheet resistivity test wafers. Figure 3.6 shows tool’s repeatability performance using bare backside (ε=0.6) Arsenic control wafers. At 1025 C for 20 seconds, Sheet resistivity varies from 56.8 to 59 ohms/square in 20 control runs. Figure 3.7 shows within wafer uniformity averages about 1.5-2 ohms/square translating
into about 1.5-2.5 C variation across the wafer. Wafer to wafer variation is about 0.5-1.2 ohms/square translating into 0.8-1.5 C of temperature variation with exclusion of implant non-uniformity. Arsenic control wafers are sensitive for anneal temperature of 1000 C or higher. Temperature sensitivity of Arsenic controls is about 0.7 ohms/sqare/C.

To monitor production processes requiring anneal temperature around 900-950 C, sheet resistivity measurements of Boron implanted controls are used. Temperature sensitivity of Boron wafers is about 2.2 ohms/square/C. Figure 3.8 shows Tool A’s performance in a repeatability study using Boron implanted control wafers. Since these controls are more sensitive to temperature change, they can be accurate indicator of tool’s performance in terms of temperature variation across the wafer. Figure 3.9 shows within wafer uniformity of 4-6 ohms/square. This is about 2-3 C variation across the wafer with exclusion of implant non-uniformity. Run to run variability is about 2-3 ohms/square giving rise to 1-1.5 C temperature variation.

Thus, for soak anneal processes (longer anneal times), Boron and Arsenic implanted control wafers indicate excellent within wafer uniformity and run to run variability. This can be attributed to single sided heating, wafer rotation with nominal speed of 150 rpm, in-situ emissivity measurement, and sensitivity of the pyrometer at wide range of wafer temperatures.
Titanium deposited wafers were also tested for existence of any oxygen leak in the RTP process chamber. This was tested visually for any discoloration on the wafer. Since this system operates under low pressure (below atmospheric), it is quite feasible to do low temperature metal silicidation processes ranging from 400-700 C for CoSi$_2$ and TiSi$_2$ formation.

**Spike Anneal:**

As the size of the transistor is decreasing, all physical dimensions such as gate oxide thickness, source/drain junction depth, contact via sizes are becoming smaller. For USJ (Ultra Shallow Junction) formation, spike anneal becomes a necessity that provides activation of dopant atoms with minimum diffusion. Spike anneal performance of Tool A has been tested using Arsenic implanted wafers. Standard bare silicon wafers were used at anneal conditions of 1125 C with ramp rates of 250 C/sec and 70-90 C/sec of ramp down rate. Dwell time for spike anneal at the nominal temperature was less than one second.

Figure 3.10 shows spike anneal performance of Tool A using standard bare Si Arsenic implanted controls. Wafer to wafer and run to run repeatability is about 0.8-1 ohms/square. The sensitivity of Arsenic wafers at spike anneal condition is about 0.5 ohms/square/C. Thus, run to run repeatability can be translated as 1-2 C of variation in temperature. Within wafer uniformity is substantially higher than soak anneal uniformity. As shown in Figure 3.11, spike anneal within wafer uniformity is about 4-6 ohms/square which translates into 8-12 C of temperature variation.
Emissivity Independence:

Emissivity independence test was done using wafers with different backside emissivities. These wafers were prepared using proprietary processes and had different thickness of poly Silicon and Oxide on their backside giving rise to emissivities values of 0.2 to 0.8. Table 3.1 and Table 3.2 show Tool A’s performance in terms of emissivity independence. Emissivity independence study was done with soak anneal and spike (short anneal time) anneal processes using Arsenic implanted wafers with different backside film characteristics.

Soak Anneal Emissivity Independence:

Table 3.1 shows the result of emissivity independence testing for Tool A. Sheet resistivity of high (0.8) and bare backside wafers were comparable averaging at about 58 ohms/square. But low (0.2) emissivity wafer has higher sheet resistivity of 60 ohms/square. There seems to be an occurrence of temperature undershoot as low $\epsilon$ wafers are colder (higher Rs means low anneal temperature) than high $\epsilon$ wafers. There seems to be a potential temperature difference between high and low emissivity of about 2.2 ohms which is about 3 C of temperature variation.

This shows that one must be careful in selecting process temperature for actual production. One must know approximately the backside emissivity of product wafer when wafer comes to annealing step. If emissivity is too low (0.2), it can be an issue in terms of temperature matching.
Spike Anneal Emissivity Independence:

Similar to soak anneal emissivity independence testing, spike anneal emissivity independence was also tested using wafers of different backside films. Table 3.3 shows results of these testing.

High, low and bare backside wafers were annealed using target temperature of 1125°C. Sheet resistivity values of high emissivity and bare backside wafers were in agreement. However, low emissivity (0.2) wafers had higher non-uniformity across the wafer. The difference between high and low emissivity wafer was about 6-8 ohms/square variation across the wafer for low emissivity wafers. This difference may be accounted from radial variation of oxide/poly backside thickness.

3.3 RIPPLE BASED RTP SYSTEM:

3.3.1. System Overview

Tool B utilizes ripple pyrometry for temperature measurement and control. It uses extensive amount of quartzware in the process chamber for provision of gas handling, wafer rotation, in-situ oxygen control, and optimized process performance. This system consists 58 lamps, 27 on the top and bottom and two on each side of the chamber. There exist an independent lamp controller (ILC) to control each lamp and to enhance within wafer uniformity by adjusting lamps individually.

In this setting, wafer resides on quartz pins and is surrounded by edge-guard ring for center to edge temperature control. Wafer is isolated from chamber and lamps by quartz plates on all sides. Temperature of the process chamber is controlled by cooling water. Temperature of the quartzware is controlled by air cooling.
Temperature Control and Measurements:

Ripple pyrometry uses sensors to receive time-dependent radiation signals from the wafer and from the heating lamps. Main advantage of this system lies into its inherent ability to compensate for different backside emissivities.

The ripple signals received by the sensors are assumed to originate from the radiation produced by the heating lamps, because thermal diffusion in Silicon is sufficient to damp out surface temperature oscillations. The pyrometer hardware and software are capable of extracting signals from the wafer and lamps. Wafer and lamp intensities are used to extract backside emissivity value of the wafer. The effective emittance of the wafer is given by a function $e(R) = 1 - R$ in regime where transmission of radiation through the wafer can be neglected. Wafer temperatures are computed from the Plank’s Law. Figure 3.3 shows process chamber of ripple based RTP system.

3.3.2. Results and Discussion

Tool B shows 1-1.5 ohms/square run to run variation for Arsenic control wafers on soak anneal recipes. Figures 3.12 to 3.17 outlines the results for Tool B's performance on soak and spike anneals including emissivity independence testing. Run to run variation of 1-1.5 ohms/square translates into about 2 C of temperature variation. Within wafer uniformity on Arsenic control wafers ranges about 2-3 ohms per square which is about 3-4 C of temperature variation. Arsenic wafer has sensitivity of 0.7 ohms per square per C. Arsenic controls were annealed at 1025 C for 20 seconds in 0.1 slm of Oxygen. Boron wafer averages about 231 ohms per square on standard anneal tests at 950 C for 20 seconds in Nitrogen ambient. Boron controls show 4 ohms/square and 5-6
Spike anneal tests were run using Arsenic based controls at 1125 C for less than one second of dwell time at the peak temperature. Specified ramp up rate and ramp down rates were 250 C/sec and 60-70 C/sec respectively. Arsenic wafer averaged about 71 ohms per square as measured by RS 75 Prometrix tool using 121 sites with 3 mm of edge exclusion. Run to run variation was about 1-1.5 ohms per square. The sensitivity of Arsenic spike controls was about 0.5 ohms/square/C. This translates into 2-3 C of run to run temperature variation. Within wafer uniformity was about 4-5 ohms/square which translates into 8-10 C of temperature variation.

Table 3.2 and Table 3.4 show emissivity independence test results using Arsenic implanted wafers with different backside emissivity ranging from 0.2 to 0.8. Tool B showed sheet resistivity difference of two ohms/square between high and low emissivity wafers for soak and spike anneal processes. Increased pyrometer oscillations were also observed on low backside emissivity wafers which may be caused by wafer rotation and non-uniformity of backside film (oxide/poly Silicon) thickness.

3.4 HOT LINER BASED RTP SYSTEM

3.4.1. System Overview

Hot Liner technology makes an effort to control wafer temperature independent of its backside emissivity. Hot Liner is a silicon nitride coated silicon wafer which is permanently installed in the process chamber, immediately below the wafer. The pyrometer, which is calibrated to device wafers, views the constant emissivity Hot Liner to produce repeatable temperatures regardless of their backside emissivity. 

30
The assumption that is made here is that silicon nitride coated Hot Liner harnesses all the wafer radiation which is eventually detected by the pyrometer viewing the Hot Liner. The process chamber design includes the use of quartz tube for gas inlet and wafer isolation. The process chamber consists of 38 lamps as shown in Figure 3.4. The chamber design is shown in Figure 3.5. Wafer resides on quartz pins in quartz tray which also includes gas distributor plates. Wafer is surrounded by edge guard ring to minimize center to edge non-uniformity.

3.4.2. Results and Discussion

Tool C qualifies as a tool to be used for technologies above 0.25 µm due to its poor temperature uniformity and lower ramp rates. This quality stems from the existence of Hot Liner increasing the thermal mass of the system and makes it impossible to heat faster. Maximum ramp up rates and ramp down rates achieved in this system are 50-70 C/sec and 20-30 C/sec respectively.

Tool C averages about 58 ohms/square on Arsenic implanted control wafers. Run to run temperature variation is about 6-7 C on soak anneals. With wafer temperature variation is about 8-10 C. Figures 3.18 and 3.19 outlines its performance.

Due to lower ramp rates, spike anneal is limitation of Tool C which is based on Hot Liner technology. 50-70C/sec and ramp down rates of 20-30 C/sec.

3.5 Comparison of three RTP systems

IC manufacturers have to consider many details before deciding to buy a particular tool set for production. Some of the variables involved in this decision making
are throughput of the tool set, proven process capability on control wafers and device wafers, total amount of fab area occupied, reliability, ease of troubleshooting and most important of all cost of ownership.

This section compares three RTP system mentioned previously in terms of their process capability and performance on implanted control wafers, throughput, and cost of ownership. It also outlines main advantages and disadvantages associated with each system and also relates how each system specifically meets manufacturer's needs.

Tool A is the most sophisticated system of all in terms of amount of hardware involved in temperature control system, and lamp heating system. This elaborate design of honeycomb lamp pattern with multiple pyrometer viewing the backside of the wafer significantly increases the cost of ownership approximately three to four times as of Tool B. Tool A's performance is equal to Tool B on Arsenic and Boron implanted test wafers as shown by similar within wafer uniformity, and emissivity independence testing on soak and spike anneals. Throughput of Tool A is 2-2.5 times more than of Tool B. Tool A consists of three separate chamber under load lock system sharing common wafer handling section. However, Tool B has only one process chamber and has throughput of 30-40 wafers per hour on standard soak anneal recipes.

Tool A and Tool B meet the challenges and requirements for tighter within wafer uniformity and minimum run to run repeatability. Tool B performs better than Tool A to a smaller extent in run to run repeatability which is about 0.8 ohms/square and 1.1 ohms/square on Arsenic soak anneal test wafers respectively. One of the advantages of Tool A is that Silicon wafer is always opaque to the pyrometer even at low
temperatures such as 400-700 C. This feature is not available in Tool B due to the long operational wavelength of the pyrometer causing no signal response in low temperature regime of 400-700 C for bare Silicon wafers.

Tool C compared to previous two systems belongs to older technology due to its lower ramp up and ramp down rates and poor control over within wafer uniformity. Increased thermal mass due to the introduction of Hot Liner makes spike anneal an impossibility for this tool. Also the temperature measured by the pyrometer in not the wafer temperature but Hot Liner temperature. To match this tool set to previous two toolsets, temperature offset must be taken into account. This is due to the existence of two different types of temperature control system. Throughput of Tool C is lower than Tool A and B about 25 wafers per hour. Cost of ownership is almost half of the cost for Tool B. It is a reliable system from maintenance standpoint due to less amount of preventive and annual maintenance. It could be an ideal tool for technology above 0.25 um. But as we go below 0.25 um towards 0.1 um, tool sets similar to A and B will be needed for better in-situ temperature control and increased within wafer and wafer to wafer uniformity.
SUMMARY

Rapid thermal processes play a crucial role in fabrication of next generation CMOS. RTP systems has unique advantage of being single wafer processors with capability of advanced gate dielectric deposition, spike anneal for ultra shallow junction applications, and low temperature metal anneals.

To meet these challenges, modern RTP systems have developed advanced non-contact based temperature control systems which can compensate for different backside emissivity of product wafers. Implementation of wafer rotation in these systems has helped significantly in improving within wafer uniformity required for smaller devices. The evaluation results for three different RTP systems can be summarized as follows:

i) Tool A: Tool A has higher cost of ownership due to its elaborate multiple input and multiple output based temperature measurement and control system. It also has increased number of lamps for temperature compensation in radial fashion. Tool A performs 1-2 C and 2-3 C of temperature variation for soak anneals on Arsenic and Boron implanted control wafers. For Arsenic spike anneal wafers, Tool A shows about 1-2 C of run to run repeatability and has difference of two ohms/square between high and low emissivity wafers. Within wafer spike anneal uniformity is about 7-9 C.
ii) Tool B: Tool B has one fourth of cost of ownership as of Tool A. It performs equivalent to Tool A in soak and spike anneals but has slight better run to run repeatability on sheet resistivity control wafers. It also shows same magnitude of difference in sheet resistance between high and low emissivity wafers as Tool A.

iii) Tool C: This tool qualifies to run older technology above 0.25 um due to its poor within wafer uniformity performance and poor ramp up and ramp down rates.
REFERENCES


BIOGRAPHICAL SKETCH

Vaibhav Trivedi was born on March 15, 1978, in India. In 1996, he joined the Department of Chemical Engineering at University of Florida. He graduated in 1999 with Bachelor of Science in Chemical Engineering with High Honors. He worked at Lucent Technologies from May 1999 to Sep 2001 as process engineer in wet etching, front end and back end cleans, Ion Implantation, and Rapid Thermal Processing. In 1999, he started his graduate studies with Department of Material Science and Engineering at University of Florida as a FEEDS student.
Table 1  Tool A: Soak Anneal Emissivity Independence Testing

<table>
<thead>
<tr>
<th>Emissivity of the Test wafer</th>
<th>Average Resistivity</th>
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<th>ohms/square</th>
<th>ohms/square</th>
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Table 2  Tool B: Soak Anneal Emissivity Independence Testing

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Table 3 Tool A: Spike Anneal Emissivity Independence Testing

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Table 4 Tool B: Spike Anneal Emissivity Testing

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Figure 3.6: Tool A: Sheet Resistivity Averages (Ohms/square) of Bare Silicon Arsenic Control Wafer Soak Anneal Runs

Figure 3.7: Tool A: Within wafer Range (Ohms/square) for Bare Silicon Arsenic Control Wafer Soak Anneal Runs
Figure 3.8: tool A: Sheet Resistivity Averages (Ohms/square) of Bare Silicon Boron Control Wafer Soak Anneal Runs

Figure 3.9: Tool A: Within Wafer Range (Ohms/square) for Bare Silicon Boron Control Wafer Soak Anneal Runs

Figure 3.10: Tool A: Sheet Resistivity Averages (Ohms/square) of Bare Silicon Arsenic Control Wafer Spike Anneal Runs
Figure 3.11: Tool A: Within Wafer Range (Ohms/square) for Bare Silicon Arsenic Control Wafer Spike Anneal Runs

Figure 3.12: Tool B: Sheet Resistivity Averages (Ohms/square) of Bare Silicon Arsenic Control Wafer Soak Anneal Runs

Figure 3.13: Tool B: Within Wafer Range (Ohms/square) for Bare Silicon Arsenic Control Wafer Soak Anneal Runs
Figure 3.14: Tool B: Sheet Resistivity Averages (Ohms/square) of Bare Silicon Boron Control Wafer Soak Anneal Runs

Figure 3.15: Tool B: Within Wafer Range (Ohms/square) for Bare Silicon Boron Control Wafer Soak Anneal Runs

Figure 3.16: Tool B: Sheet Resistivity Averages (Ohms/square) of Bare Silicon Arsenic Control Wafer Spike Anneal Runs
Figure 3.17: Tool B: Within Wafer Range (Ohms/square) for Bare Silicon Arsenic Control Wafer Spike Anneal Runs

Figure 3.18: Tool C: Sheet Resistivity Averages (Ohms/square) of Bare Silicon Arsenic Control Wafer Soak Anneal Runs

Figure 3.19: Tool C: Within Wafer Range (Ohms/square) for Bare Silicon Arsenic Control Wafer Soak Anneal Runs
Figure 3.1: Tool A: Schematic Diagram of RTP chamber and lamphead

Figure 3.2: Tool A: Temperature Control System
Figure 3.3: Tool B: Furnace and Pyrometer Schematics (5)
Figure 3.4: Tool C: Arrangement of Lamps

![Diagram of Tool C: Arrangement of Lamps]

Legend:
- Chamber door
- Side lamps
- Upper lamps

Note: Numbers 1 to 38 correspond to specific lamp positions.
Figure 3.5: Chamber Overview (7)